

10th Workshop on Crystalline Silicon Solar Cell Materials and Processes

Extended Abstracts and Papers

Workshop Chairman: B. L. Soporì

Program Committee:

J. Gee, J. Kalejs, T. Saitoh, R. Sinton, M. Stavola,
D. Swanson, T. Tan, E. Weber, J. Werner, and
B. L. Soporì

*Copper Mountain Resort
Copper Mountain, Colorado
August 14-16, 2000*



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National Renewable Energy Laboratory

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Silicon Photovoltaics – 10 Years of Progress and Opportunities for the Future

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Tremendous progress has occurred in the science and technology of silicon photovoltaics during the past decade. For the first time, Si-PV has become a profitable business and companies are experiencing a backlog in module delivery. New increases in the production capabilities are being implemented by nearly all Si-PV companies to meet the increasing demands. The total worldwide sales of the PV modules in the last 10 years reflects a production increase of about 20% per year. While the production volumes have increased steadily, the module costs have declined because of increased production and improved solar cell efficiencies.

The PV industry has now established itself as a viable and profitable industry. At more than 80% of the sales, silicon continues to have the major share of the PV market. Silicon solar cells used in the current commercial modules have efficiencies of 14%-15%. These high efficiencies are the result of implementing in-depth knowledge of the low-cost substrate properties and use of advanced solar cell processing acquired through well-defined research. An important area of research during the last 10 years has been toward understanding defects and impurities in silicon. This knowledge has enabled a significant improvement in the quality of the low-cost substrates. Processing of these substrates using gettering and passivation to mitigate their deleterious effects on the cell performance have led to high-efficiency cells.

It is very interesting to note that 10 years ago very little was known about the physics of the post-growth material-quality upgrade. Perhaps a lack of a detailed information prompted researchers to stretch their imaginations to visualize processes that could remove impurities and annihilate defects in the material during subsequent solar cell processes. It is remarkable that processes actually work. Much of this credit goes to teams of researchers and research programs that embarked on the study of impurity gettering and defect passivation. As a result of the worldwide research efforts, a wealth of knowledge has been acquired and applied to improve the material quality as a byproduct of solar cell fabrication. This workshop has been instrumental as a forum to consolidate research results, propose new ideas, and define directions for research and development.

In the laboratory, new understanding of impurity effects and impurity control in cell processing, effective methods of light-trapping, control of interface recombination, and new understanding of metallization processes, have led to record efficiencies on high-quality single-crystal FZ and CZ materials. This understanding has also favored a push toward thin and thin-film solar cells.

Although much progress has been achieved, more challenges lie ahead. These challenges are apparent in the PV Roadmap; these challenges will appear in the entire gamut of crystal growth, fundamental physics of impurities and defects, to engineering aspects of solar cell production.

Improving commercial cell performance toward 18%—20% is a crucial step that will require novel concepts on impurity-defect interactions. Recent studies show that defect clusters are accompanied by impurity precipitation. The precipitated impurities are hard to getter, leaving regions of low performance in a solar cell. Clearly, it is imperative that feasible processes for impurity dissolution and gettering must be developed. Alternately, material quality of the substrates must be improved—interestingly, an approach advocated by some researchers in the field. Further understanding of impurities and defects is needed to address whether the precipitated impurities can be isolated by passivation.

Thinner cells, light-trapping, commercial metallization schemes for improving cell fill factor, high throughput processing, process controls, and automation will be essential. Sawing thinner wafers with reduced kerf losses (using wire saws) has been a major factor in reducing the cell cost. Solar cell process-monitoring poses its own challenges. Development of high-speed methods for measurement of relevant parameters on large-area, rough wafers/cells will play an important role in process monitoring. Going to 100- μm thin wafers and cells will be a daunting challenge. The PV industry will need dedicated equipment and equipment manufacturers to support this field. These are opportunities for scientists, engineers, and entrepreneurs to participate in making PV a lasting resource.

This workshop reflects a strong determination by the PV community toward meeting these challenges. Willingness of the workshop attendees to participate in the crucial discussions, the efforts of the Program Committee to emphasize the topics of importance to industry in a judicious manner, and devotion of speakers who spent much time for preparation of review talks, have contributed to the success of the workshop. The theme of this year's workshop is very timely. This theme complements the recent establishment of the PV Industry Roadmap. The workshop also includes two special sessions, Metallization and Interconnections, and Characterization Methods, that are aimed at stirring up new ideas to deal with bottlenecks in these areas.

Making the Photovoltaic Industry PV Technology Roadmap: Issues and Next Steps

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The photovoltaic (PV) community is showing signs of a new willingness to collaborate and form partnerships for equipment design and product standardization to speed development and reduce costs. A decade ago, as NREL was hosting the first workshop on silicon point defects and processing, the microelectronics industry was experiencing a business challenge that prompted similar willingness to open-up in some areas that had been proprietary and to explore opportunities for joint pursuit of pre-competitive technology, research, and equipment design. Scientist and engineers pushed back from the daily grind of improving the immediate product generation to examine the challenges of developing the advanced technology needed to sustain Moore's Law. In 1995, the near term success of a company might hinge on protecting proprietary knowledge believed important to be first to achieve 0.35 micron features on 200mm wafers. The same participants could open up and share their vision in the collective effort to identify pathways, materials, and equipment needs to achieve 0.07 micron devices on 400 mm wafers in 20 years. Focusing attention on this long-term target likely contributed to the community's success in developing the semiconductor technology roadmap. The roadmap and the industry interactions that created it helped to frame domains for collaboration and for competition. As a result, the microelectronics business and technology accelerated their rate of progress.

Human nature drives our focus to areas of contention. For experts in a field we may agree on 80% of the issues in our area, but the intrigue is in the last 20%. This works to the detriment of delivering a clear message to the general public or policy makers. For example, the growing body of data and understanding of trapping energy by green house gases is well accepted among atmospheric scientist. The intriguing issues revolve about the earth's response. Where will it be hotter? Is the response likely to be chaotic or gradual? Is the thinning of the ice caps evidence or part of some other cycle? Focus on these questions makes excellent science and lively debate, but obscures the collected data on temperatures, temperature fluctuation, CO2 concentrations and similar consistent findings. The critical issue for the PV Roadmap is to present the plausible scenario for growth to a scale of measurable contribution of energy to meet global demand. This has been obscured by our debate over the merits of the various technologies and products. After we have shown how PV will make a difference, then we can argue among ourselves whether there will ever be PV central station power or what portion of the 2 billion people without electricity will adopt PV.

While PV has not established industry wide production patterns like the microelectronics industry—new product generations with smaller feature size every 2.5 years, upgrade production equipment for larger wafers every 5—we have established a pattern of steady production growth and cost reduction. It should surprise no one skilled in arithmetic

that if the PV industry maintains a compound annual growth rate of 25%, it will be a very big business in 20 years. Even still, the effect of compounding whether in calculating the full cost of a mortgage, the projected value of a retirement account, or the size of a PV industry surprises the majority of humans. U.S. PV production will exceed 6 GW annually by 2020. It is unlikely that lighted highway signs will require this much product. The structure of the PV market in the U.S. will need to change substantially in 20 years if the projected growth in domestic PV production is to be sustained. The framework for the PV Industry Technology Roadmap targets faster growth of domestic markets such that half of the PV production is consumed within the U.S. (versus 30% today). This projection has aspects of both cause and effect. The result is that PV installations will account for 15% of the growth in U.S. electricity generating capacity in 2020.

PV has established an experience curve of about 80%. Costs drop by about 20% when the cumulative production experience is doubled. Combining this with the projection for cumulative module shipments points to about a 5-fold reduction in the cost of PV systems. At that point, PV can plausibly compete at wholesale costs in some utility systems. Thus, the domestic market is seen as composed of about half in building integrated (BIPV) and other distributed generation, a third continuing in the DC and AC value added and enabling applications, and a sixth into utility-scale, grid-connected systems. This vision of segmentation of the maturing market for a big PV industry leaves open the possibility for many viable technologies. In some cases, systems with far different operating characteristics and costs structures may co-exist without competing, e.g. concentrating PV ground mounted systems and BIPV.

The plausibility of the Roadmap will depend on the past performance of the PV industry in addressing its problems. The way that the PV industry deals with the challenge of developing supply of silicon feedstock will be an important learning experience and potentially a valuable demonstration the community's business prowess. As PV grows, silicon feedstock is the first of many supply bottlenecks. Today we consume about 10% of the silicon used in electronic devices. Projecting growth and utilization efficiency improvements for both the microelectronics and PV industries, by 2020 PV will demand about a third of the silicon and certainly require some dedicated supply channels. Without change in the encapsulation design, 6 GW production will consume the output of 4 float glass plants each producing 600 tons of glass daily. PV modules will require about 10% of the U.S. glass production. Glass suppliers will be investing \$100M to install a 5th plant to meet demand growth. Their willingness to make that investment will in some part be determined by the PV industries' performance on the Silicon feedstock issue.

During the PV Roadmap Workshop in June 1999, the panel examining manufacturing issues discovered that a major supplier of EVA to the PV industry produces formulations to eight different specifications. This and other materials would benefit in cost and availability if the industry worked together to establish some product standards.

If PV growth is to be sustainable, the capital cost of production facilities must be reduced. A few PV companies today view the design of custom equipment as critical to their competitive position as module manufacturers. Such an operation runs counter to several paradigms for business success. All PV companies have experienced some difficulty in purchasing equipment built to specification. Very few pieces of production equipment can be seen as standard items. Our industry creates too much of its technology in a proprietary way. Companies do not go outside their organizations for development, frequently resulting in duplicate R&D within the industry. This mode of operation must change if the industry is to grow rapidly. The first step in reducing capital cost for high-throughput equipment and facilities will be to make more effective use of equipment development dollars through partnerships and joint development.

The next steps in converting the current report of the PV Roadmap Workshop into a PV Industry Roadmap will be quite challenging. The semiconductor industry was able to focus their attention on one type of chip to guide the development of equipment, materials, and processing paths. In PV there does not seem to be such a common point for focus. It will be difficult to avoid competition among the possible pathways, yet to succumb to these debates (as is our culture) will certainly weaken the case showing PV's growth as a significant energy supplier. The next steps should be taken with a view toward using the process of developing a roadmap as a means to identify opportunities for partnering for R&D, product standards, and equipment. If the result is a cogent document that supports each part of the community, then we will be well on the way to creating a business that is big enough for all to prosper.

Ten Years of Progress – x-Si Material R&D and Trends in Wafer Supply Development in the USA: 1990-2000

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The past decade in R&D in crystalline silicon materials has been associated with the development and expansion of wafer supplies in the USA at an unprecedented pace. Established methods of production based on CZ growth and ingot casting and a new generation of ribbon technologies both have flourished. Several new technologies have now reached maturity with deployment of multi-MW manufacturing facilities in the USA, and are starting to give strong competition to established wafer production methods. The USA has become the world “capital” of ribbon technologies, in particular, with the start up of manufacturing on a MW scale of Edge-defined Film-fed Growth (EFG), String Ribbon, Dendritic Web, and Silicon Film. A summary of the changes in status of various technologies in the US over this decade is given in the table below. I present my estimate of US-based wafer production capacity that is currently on-line and being planned for the next year. We can project that in perhaps as little as a year we will have well in excess of 100 MW of crystalline silicon wafers being produced in the US, and more than a third of this from ribbon technologies – a truly remarkable development in 10 years!

Wafer Process	1990		2000	2001
	Status	Level		
Conventional				
CZ	Production	10 MW	35-40 MW	> 50 MW
Ingot Casting	Production	5 MW	15-20 MW	> 30 MW
HEM*	R&D	< 0.1 MW	Production > 10 MW*	> 20 MW*
Ribbons				
EFG	Pilot	1.5 MW	Production – 12 MW	> 20 MW
ESP/String Ribbon	R&D	-	Pilot < 0.5 MW	Production - 10 MW
Dendritic Web	Pilot	0.5 MW	Pilot ~ 0.5 MW	Production - 2 MW
Silicon Film	-	-	Pilot - 2 MW	Production > 5 MW

* This production capacity is not all US-based.

The NREL Silicon Defect Workshop agenda coincidentally and by design also has grown and flourished along with the US x-Si wafer industry in this decade. It is rewarding for those who have participated in these Workshops to look back in retrospect, to review progress, and to express satisfaction about contributions made by the scientific program of the Workshops to aiding the growth of wafer manufacturing. I will review in this paper my own personal highlights in the crystal growth area over this decade of Workshops. I will also look in my crystal ball for what may be in store for the future.

Point defect topics kicked off the Workshops in Keystone in 1990, and this first Workshop initiated a decade-long investigation of point defect manifestations in solar materials. Although thoroughly studied in the semiconductor world, most of the photovoltaic world was relatively ignorant of how they influence material properties. Point defect models have added greatly to understanding of material characteristics in

solar materials. In retrospect, I cannot see a singular impact of point defect understanding on the improvements of EFG material and its manufacturing methods. It almost is the opposite. Point defect understanding and theory multiplied the possibilities and explanations for each and every puzzling experiment. And there are far more puzzling results in the complex solar materials than simple explanations. Crystal growth is what it is, there are very few “adjustable” parameters. Generally, the paramount objective of growth process development for solar materials was to push toward higher productivity systems. This constrained opportunities to manipulate point defects during growth. Point defect theory made greater contributions in cell processing, particularly in understanding of gettering. The most important result for me, as the world of point defect phenomena opened up in EFG material, was the demonstration, time and time again, that solar silicon is “normal” silicon - point defect phenomenon follow the same rules, albeit in a more complex environment. Contrasting the varying behaviors of carbon and oxygen, together with point defects, and how they may be controlled in crystal growth, were also topics of these early meetings which helped me understand EFG material.

One highlight of this early period for me was the lively discussion and controversies at the 4th Workshop in connection with initial results I presented on Fe-B and Cr-B pairs in EFG material. This Workshop seemed to mark a transition to new topics. The 5th Workshop and following ones featured more prominently transition metal impurities, extended defects and devices. Discussion of the origins of electrical activity of dislocations in crystal growth and the role of transition metals, gettering and passivation, took over the stage in study of EFG material, as well as the rest of the solar community. A major step forward in leading to improvement of EFG material was gaining understanding of and distinguishing bulk lifetime changes that could be related to fast diffusing impurities such as Fe and Cr, from those caused by the slow diffusers Ti, Mo and V. Control and elimination of transition metals in crystal growth has been a central activity at ASE Americas. The knowledge gained in this area from Workshop interactions has contributed significantly to as-grown EFG material improvement over the decade. Cu has had an extensive exposure, but its impact on influencing EFG as-grown material and solar cell properties has not been demonstrated to be significant. An outgrowth of interest in study of electrical activity in wafers was bulk lifetime measurement. Several satellite meetings devoted specifically to measurement techniques have followed. In spite of much progress, meaningful measurement of as-grown electronic quality in many solar materials, such as EFG silicon, that can be predictors of its response to cell processing, is still elusive.

Emphasis in the past few Workshops has shifted to solar cell processing, manufacturing issues, and thin layer silicon. Crystal growth is getting less attention. This is setting the trend for the next decade’s activities. I believe this reflects the maturity of the crystalline silicon wafer industry. On account of the large projected rise in silicon feedstock requirements for the growing industry, solar grade feedstock topics have often replaced discussions on crystal growth effects on material properties and characterization. Feedstock supplies will be a hot area of activity in the next decade. Thin wafers, and high quality wafers – e.g., 20% efficiency on ribbon materials with low cost cell processing – are goals which need to be achieved in order to produce another round of large cost decreases and volume expansion in these new generation silicon wafers. We will have to wait for crystal growth to again have its day when thin silicon challenges ribbon growth.

Transition metals in silicon: the continuing story

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The history of metal impurities in silicon is almost as long as the history of silicon technology itself. The first systematic studies of transition metals in silicon were published in the 1950s. It is interesting to note that in the flood of papers on this topic published in the last 50 years, there are a few even from the earliest years that withstood the test of time and are still correct and relevant today. Some of these studies to be mentioned are the articles by Struthers (1), Collins and Carlson (2), Hall and Racette (3), and Gallagher (4). Already these early studies indicated that transition metals are impurities with very high solubility in silicon, which can significantly affect its electrical properties. Several fundamental theoretical studies, which greatly affected our understanding of impurities in silicon, such as the study of recombination activity of metal impurities by Shockley, Read, and Hall (5, 6) or the study of dynamics of iron pairing in semiconductors by Reiss, Fuller and Morin (7) also came out in the 1950s.

The first electrical studies published in the 1960s were followed by the famous EPR studies of Ludwig and Woodbury (8, 9) that put the physics of transition metals in silicon on a very solid footing. Remarkably, the pretty basic science developed in those papers remains as relevant today as it was 35 years ago. It is also remarkable that almost everything in those papers stood the test of time (maybe with the exception of the interstitial Ni that is still not yet clear). Diffusion and solubility data of impurities in silicon have been compiled by Trumbore in 1960 (10). While some of these values are out of date because of the lower level of semiconductor technology at that time, some remain valid and are used until now.

In the 1970s there was quite some confusion in the area of transition metals, e.g., with the issue of the 'thermal donors' that turned out to be Fe contamination. Invention of DLTS by Lang in 1974 (11) made studies of electrical levels associated with contaminants very fast and accurate. Several groups simply diffused transition metals and used DLTS to make catalogues of deep levels. Although this idea was extremely simple, accurate identification of the energy levels, and the microscopic nature of these levels (such as interstitial/substitutional impurities, defect complexes, etc.) took years. Experiments with rather unspecific methods such as resistivity or Hall effect measurements, the use of poorly defined specimens, contamination during diffusion treatments and uncontrolled complexing reactions resulted in a tremendous amount of data that can hardly be ascribed to specific defects and defect configurations. As an example, Graff and Pieper (12) demonstrated that the energy levels quoted for iron in silicon cover the whole band gap. The same holds for most of the other transition metals. Electrical data reported at that time have thus to be treated with care.

The understanding of transition metals in silicon got better in the 1980s. One should mention especially the studies of Graff from Telefunken (12-14), and NAA studies of solubilities of transition metals in silicon published by Weber and Riotte (15, 16). Independent from these two groups, Lemke from East Germany deserves a special mentioning. As we now know, he did a fantastic, careful job, almost un-noticed in literature as he published mostly in German (17-33) (28). The groups of Schröter (34, 35) and Feichtinger (36-41) were other active groups which are

worth mentioning although these addressed more specific problems and worked therefore in greater depth. The 1983 review article of Weber (42) summarized and systematized all data on transition metals in silicon available at that time. The fact that nearly all data presented in that review remain valid until now shows that a fairly good basic understanding of transition metals had been reached by the early 1980s.

In the 1990s we started to notice the need to go beyond the basic understanding of diffusion, solubility, lattice site and energy levels of metals obtained in the 80s. This was necessary to be able to do “defect engineering”, i.e., to affect the properties of impurities in silicon by triggering specific defect reactions and suppressing the others to minimize the effect of metal impurities on device properties. To engineer defects we had to learn more about their physics, including complexing and clustering of metals, their reactions with other defects and impurities, and kinetics of these processes. Therefore, after a period of relatively weak interest of silicon industry to fundamental research in the 1980s – early 1990s we see an increasing level of interest to fundamental research in the both silicon communities, PV and IC, which resulted in such fruitful joined efforts as the NREL research program, German DIXSI project, and SiWEDS. Implementation of copper interconnects in integrated circuit technology stimulated research of the physics of copper in silicon and resulted in a significant progress in its understanding ((43-49) to mention a few recent papers). Several new reviews on metals came out (50, 51).

In photovoltaics, transition metals are a serious concern because they are strong recombination centers and affect the minority carrier diffusion length (52-55). Additionally, precipitates of metals in p-n junction may cause shunts. Gettering of transition metals, quite efficient in CZ silicon, was shown to be problematic in multicrystalline solar cells (56-59). This was explained by either slow kinetics of dissolution of bulk microprecipitates (60), or by formation of oxides of silicides of these metals in the bulk (61). Recent research efforts sponsored by NREL indicated that improvement of the minority carrier lifetime in multicrystalline silicon and passivation of defect clusters is a complex task which requires state-of-the-art research tools and new approaches.

In summary, the story of transition metals in silicon continues after 50 years of development, and we will certainly see new exciting developments in the near future. We have basic understanding of solubility, diffusivity, and electrical activity of transition metals in silicon, and we are on our way to better understand, model, and engineer defect reactions of these metals that will enable us to minimize their effect on device performance.

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Advances in Low-Cost Multicrystalline Silicon Solar Cell Processing in the Last Decade

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Abstract

The U.S. Photovoltaic Industry Roadmap calls for an increase in low-cost Si PV cell efficiency to 16% by 2003, and 18% by 2010. This paper presents the guidelines for achieving $\geq 18\%$ efficient industrial cells through an assessment of impact of individual cost-effective design features. This paper also reviews recent progress in high-efficiency manufacturable and non-manufacturable mc-Si solar cell technologies with the aim of identifying which technologies are the most promising for the long term goal of silicon photovoltaics.

1. Introduction

Worldwide PV shipments are expected to reach 200 MW in the year 2000, with 80-85% modules made from crystalline silicon at a cost of \$3-4/watt. The module cost needs to decrease by about a factor of four to compete with conventional energy sources. Si material, cell processing, and module assembly each contribute about 45%, 25% and 30% of the cost of current PV modules made from ingot materials. Due to the high cost of Si, emphasis is gradually shifting from monocrystalline silicon to multicrystalline cast and ribbon silicon, which now account for about 45% of the market. Development of high efficiency cells on thin, low-cost materials using cost-effective technologies can significantly reduce the cost of Si PV.

Even though laboratory silicon cell efficiencies have reached 24.7%, the production cell efficiencies are only in the range of 12-15%. Unfortunately, laboratory cells are too expensive and industrial cells are not efficient enough to meet the target of \$1/watt for PV modules. Detailed examination of the laboratory and industrial cells suggest the efficiency gap between the two can be reduced by cost effective implementation of advanced design features such as a) effective front and back passivation b) effective light trapping by front surface texturing and a good back surface reflector c) reduced shading and contact recombination d) selective emitter formation and e) higher diffusion length to cell thickness ratio. Reasonable efficiency targets for industrial cells are 18-20% for monocrystalline silicon and 16-18% for multicrystalline silicon. This paper shows a roadmap for achieving $\geq 18\%$ efficient industrial cells and highlights recent advances in silicon technologies that can get us there.

2. Guidelines for Achieving Manufacturable High-Efficiency Si Cells on Low-Cost Materials

Model calculations were performed using the PC1D program to establish a roadmap for achieving $\geq 18\%$ efficient cells on low-cost materials with a bulk lifetime of only 20 μs . Emphasis is placed on technologies and cell designs that are practical for commercial cells, but may need further development. Figure 1 shows that a 300 μm thick 1 $\Omega\text{-cm}$ materials with a) a bulk lifetime of 10 μs b) poor front and back surface passivation ($S_f = 2 \times 10^5 \text{ cm/s}$ and $S_b = 10^6 \text{ cm/s}$) c) a poor back surface reflector (BSR) (40%) d) a single layer AR coating with no texturing e) poor screen printed (SP) metallization on a 45 $\Omega/\text{emitter}$ with 8% metal coverage, excess junction shunting ($R_{sh} = 500 \Omega\text{-cm}^2$) and a FF of 0.73-0.74, produces a cell efficiency of 12.9%. This is quite close to the average efficiency of commercial mc-Si cells today. The second bar in Figure 1 shows that

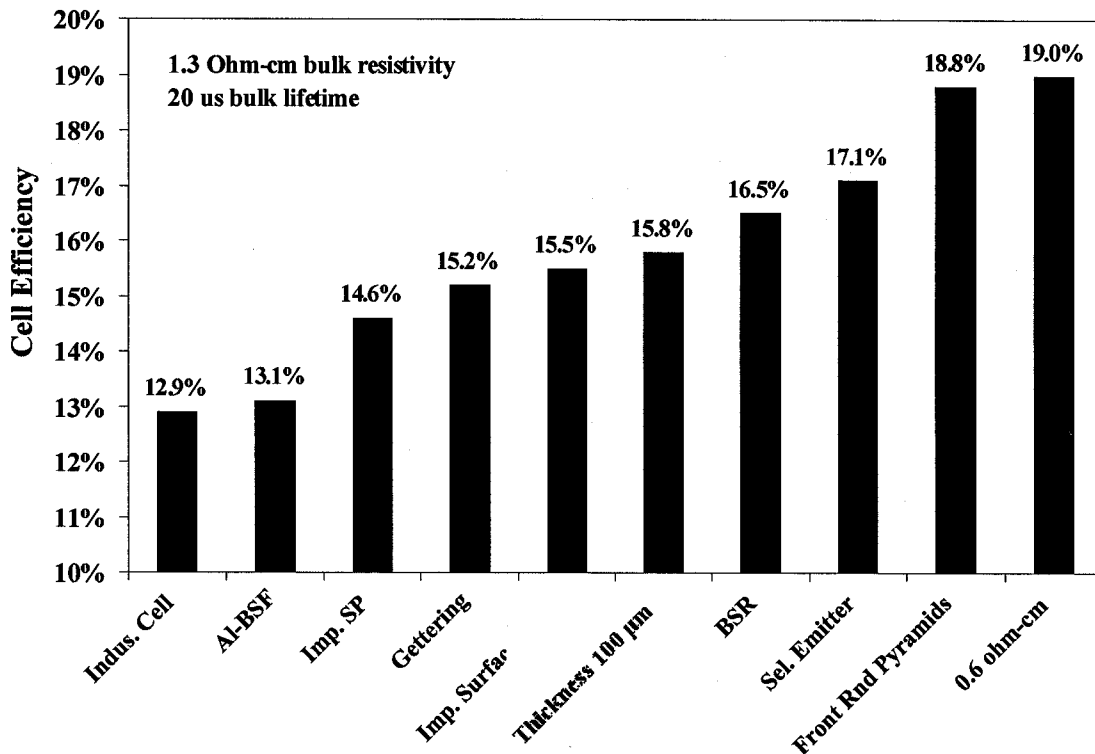


Figure 1: Incremental Improvement in Cell Performance with Manufacturable High Efficiency Technologies.

applying an Al-BSF with an S_b of 500 cm/s can improve this efficiency to 13.1%. If the SP metallization can be improved, more reasonable FF (0.78) with $R_{sh} = 10^5 \Omega\text{-cm}^2$, $J_{02} = 5 \text{ nA/cm}^2$, $R_s = 0.6 \Omega\text{-cm}^2$, and metal coverage of 6%, a significant improvement in efficiency to 14.6% can be achieved. Improvement of the bulk lifetime from 10 μs to 20 μs by appropriate gettering and passivation can improve the efficiency to 15.2%. Improving the front surface passivation from $S_f = 10^6 \text{ cm/s}$ to $3.5 \times 10^4 \text{ cm/s}$ raises the efficiency to 15.5%. Reducing the cell thickness to 100 μm has no adverse effect on cell performance if the back surface reflector is 70-80%. Thinning the cell actually improves

the efficiency by 0.3% and the addition of a good BSR raises the cell performance to 16.5%. This strongly endorses the use of thinner silicon for cost reduction. The next bar in Figure 1 shows that the formation of a selective emitter for SP cells with $85 \Omega/\square$ between the grid line and $\leq 45 \Omega/\square$ underneath the grid, coupled with good front surface passivation, $S_f = 7500 \text{ cm}^2/\text{s}$, can raise the efficiency to 17.1%. Finally, if we can raise the bulk lifetime in $0.6 \Omega\text{-cm}$, low-cost Si to $20 \mu\text{s}$ through an understanding of the dopant defect interaction, then efficiency of 19.0 % can be achieved. Incorporation of a double layer AR coating can raise the efficiency beyond 19%. The following sections show the advances made in Si processing which incorporate the above high efficiency features on mc-Si in manufacturable as well as non-manufacturable fashion.

2.1 Advances in Si Technology for Achieving High Efficiency Cells on Low-Cost Materials

Multicrystalline cell efficiencies have increased steadily over the past two decades (Figure 2). These gains have been brought about by improved material quality and advanced cell processing. The progress in mc-Si cell efficiencies has been subdivided into three categories: a) small area ($1\text{--}4 \text{ cm}^2$) laboratory cells using non-manufacturable and expensive technology and b) large area cells ($\geq 100 \text{ cm}^2$) using the combination of manufacturable and non-manufacturable technologies and c) large area cells with technologies that may become manufacturable. In addition, Figure 2 shows that large area cells using well established, cost-effective technologies, currently are in the 12–14.5% range.

The highest mc-Si cell efficiency (19.8%) on a textured surface has been reported by UNSW using $1.2 \Omega\text{-cm}$, $260 \mu\text{m}$ thick, Eurosolare cast mc-Si in conjunction with well documented PERL cell technology [1]. This technology involves multiple high temperature and photomask steps to achieve a phosphorus diffused selective emitter, local boron back surface field, excellent front and back oxide passivation with point contacts on the rear, front and back pl contacts, and a honeycomb textured surface and formed by photolithography.

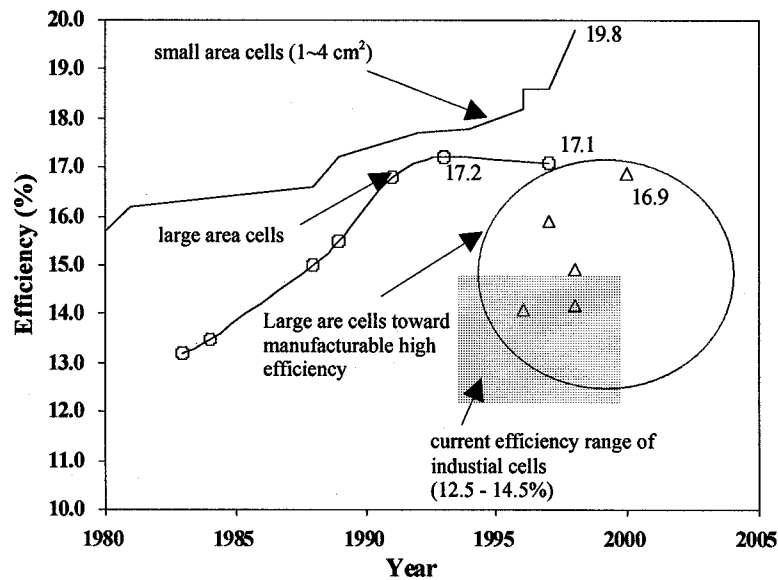


Figure 2: Progress in mc-Si cell efficiency over the past two decades.

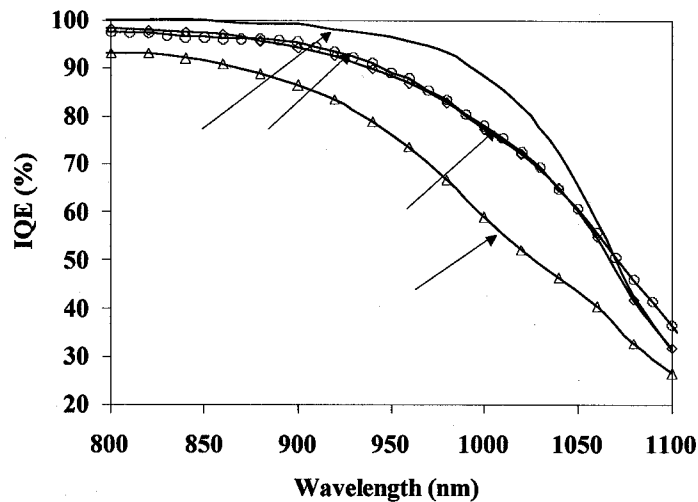
Georgia Tech reported the highest efficiency (18.6%) planar mc-Si device using a much simpler process without surface texturing, point contacts or a selective emitter [2]. Cell fabrication involved a 900°C/30 minute phosphorus diffusion on the front followed by a second high temperature step, which provided front oxide passivation, Al-BSF, and hydrogenation of defects via forming gas anneal (FGA). Front contacts were formed by photolithography and a double layer AR coating was applied. It was shown that phosphorus and aluminum gettering and FGA induced hydrogenation were able to raise the starting bulk lifetime of 10 μ s in the HEM mc-Si material to the 35-135 μ s range. LBIC measurements were used to point out that some cells were only 17% due to regions of very high electrically active dislocations and defects, which could not be removed by conventional gettering and passivation. New technologies need to be developed to eliminate such regions in order to achieve large-area high-efficiency cells. The above two cell technologies demonstrate that 18-20% cells are achievable on mc-Si provided advanced cell design features are incorporated and the bulk lifetime in excess of 20 μ s.

2.2 Recent Advances in Low-Cost Technologies for High Efficiency Cells on Low-Cost Materials

2.2.1 Screen Printed Al Back Surface Field

The second bar in Figure 1 shows that replacing an ohmic contact ($S_b=10^6$ cm/s), with a good Al-BSF ($S_b=500$ cm/s), can raise the efficiency by 0.2% even when the cell thickness is 300 μ m and the bulk lifetime is 10 μ s.

Effects are much greater on a thin device. A p-p⁺ high-low junction can be formed by Al alloying or boron diffusion. Boron BSF formation requires a long high temperature ($\geq 950^\circ\text{C}$) diffusion which may occasionally degrade the bulk lifetime in low-cost materials due to the dissolution of metallic precipitates. An Al-BSF is more desirable because it can be formed at lower



temperatures ($\leq 900^\circ\text{C}$) in a very short time (< 5 minutes). Lolgen [3] and Narasimha [4] both measured an S_{eff} value of ~ 200 cm/s from SP Al-BSF formed on 2-3 Ω -cm monocrystalline Si. However, an S_{eff} value for a SP Al-BSF on mc-Si has not yet been established. It could be somewhat higher due to the presence of defects at the p⁺-p interface. Chalfoun [5] and Narasimha [4] also showed that Al-BSF quality is a strong function of the ramp-up rate; faster the rate, more uniform is the BSF. On that basis Narasimha [4] showed (Figure 3) that an RTP Al-BSF is superior to a BSF formed in the

belt furnace, and co-firing of front and back contacts at 730°C in a belt, which results in a very poor Al-BSF. Many cell manufacturers today use co-firing to eliminate one firing step, but this comes at the expense of BSF quality.

As we move toward thinner cells (~100 μm), Al-BSF formation may warp the devices. This will require the development of a bifacial device structure with dielectric passivation on the rear with a punched through Ag or Al grid. Rohatgi et al. [6] reported a SP bifacial device with an efficiency of 17.0% on monocrystalline silicon using an oxide/nitride stack on the rear with a Ag grid. They calculated an S_b of 340 cm/s and a measured rear illuminated efficiency of 11%.

2.2.2 Improved Screen Printed Metallization

Most cell manufacturers use screen-printing today because it offers a simple, low-cost, and rapid method for metallization. However, cost and throughput gains are achieved at the expense of FF and cell performance. SP generally introduces more shadow losses and requires an emitter with high N_s , which introduces heavy doping effects and hurts surface passivation. The latter can be mitigated by selective emitter formation. In addition, some investigators [7] have demonstrated printing of grid fingers with line widths as thin as 50 μm lines using modern screens and reduced emulsion thickness. Rohatgi et al. [6] have shown a methodology for optimized SP firing scheme for a given Ag paste and achieved FF as high as 0.795 on monocrystalline silicon with 0.5 μm deep emitters. However, SP of mc-Si cells with shallow junction emitters ($\leq 0.3 \mu\text{m}$) formed by rapid belt furnace processing still show FF in the range of 0.74-0.77. This is partly due to a paste-defect interaction which leads to junction shunting during firing and increases J_{02} . Firing contacts through the SiN_x AR coating, a scheme developed by IMEC [8], reduces junction shunting and also improves bulk and surface passivation due to the release of hydrogen from the SiN_x film. There is an urgent need for an understanding and optimization of paste purity and composition, frit content, and firing scheme that can give rise to high FF (≥ 0.78) reproducibly on mc-Si cells, because the FF of most production cells are only in the range of 0.70 – 0.75.

2.2.3 Simplified Buried Contact Technology

Buried contact solar cell (BCSC) technology was developed at UNSW and is well documented in the literature [9]. Large area cell efficiencies of 17-18% on Cz and 15.8% on mc-Si have been reported using the conventional single sided BCSC technology [10]. A typical process sequence involves texturing and light n^+ diffusion over the entire surface followed by a thick passivating thermal oxide on the front and back. A 40-50 μm deep mechanical or laser grooving is performed to define grid regions. A heavy n^{++} diffusion is performed into the grooves to form a selective emitter utilizing the thick oxide mask. An Al-BSF is formed, followed by electroless plating of Ni, Cu, and Ag, while the thick oxide between the grid lines serves as a plating mask. Advantages of BCSC technology over SP include high metal conductivity, large cross sectional area and high aspect ratio for the contact grid with minimal shadow losses, and selective emitter. Since the process involves multiple lengthy high temperature steps, groove formation,

etching, cleaning, and multi-layer plating, a simplified BC process is being developed which involves mechanical grooving, texturing, a single n^+ diffusion, rear BSF, AR coating and plating. This process reduces the number of high temperature steps but sacrifices V_{oc} . Some initial runs on single crystal silicon have been made, but no results on mc-Si are yet published.

2.2.4 Selective Emitter Formation with Good Front Surface Passivation

Figure 1 shows that selective emitter for SP devices in conjunction with good front surface passivation ($S_f=7500$ cm/s) can give $\sim 0.6\%$ increase in efficiency. Heavy doping ($\leq 40 \Omega/\square$) reduces the contact resistance and junction shunting, and well passivated lighter field diffusion ($\geq 80 \Omega/\square$) improves the short wavelength response.

Ruby et al. reported on the selective emitter formation by partially etching away the heavily doped layer between the grid lines using plasma RIE followed by SiN_x deposition in the same reactor for surface passivation and AR coating [11]. This process resulted in $\sim 13\%$ efficiency mc-Si cells with some FF reduction.

A second approach involves two separate diffusions followed by alignment of the SP grid to the heavily diffused regions. This resulted in an efficiency of 16% on 100 cm^2 mc-Si using oxide passivation [13]. A third technology for selective emitter formation on mc-Si is being developed at IMEC, which involves a single step diffusion from a phosphorus dopant paste which is screen printed in a grid pattern followed by a diffusion in a tube furnace [13]. The areas under the grid are deeply diffused whereas in the areas between the grid, a shallower diffusion is obtained via gas phase transport of the dopant or autodoping. Using this technology, IMEC has recently produced 100 cm^2 mc-Si cells with efficiencies of 16.3% . The process sequence involved acidic isotropic etching, printing of phosphorus paste followed by burnout of organics in a belt furnace and selective diffusion by autodoping at 850°C in a quartz tube furnace, PECVD SiN_x deposition for surface passivation and AR coating, alignment of the SP grid to the heavily diffused regions, screen printing of Al on the back, and co-firing of both contacts. A double layer AR coating increased the efficiency to 16.9% .

A fourth selective emitter technology involves the use of self-doping Ag paste on a lightly diffused emitter. After firing this specially prepared phosphorus containing paste above the Ag-Si eutectic, a n^{++} doped Si region is formed underneath the grid by liquid phase epitaxy in a process similar to the formation of an Al-BSF. This process forms a self-aligned selective emitter where the Ag grid is self-aligned to the heavily diffused regions. This process has recently produced $13\text{-}14\%$ efficient $100 \mu\text{m}$ thick selective front surface field, n^+-n-p^+ Dendritic Web cells and $15\text{-}16\%$ selective emitter cells on p-type monocrystalline Si at Georgia Tech.

2.2.5 Surface Texturing

Figure 1 shows that surface texturing can produce a significant improvement in cell efficiency by reducing reflection, increasing carrier collection, and enhancing light

trapping by internal reflection. The best texturing has been achieved by inverted pyramids, but it is not manufacturable because it involves lithography. Random pyramids have been realized on (100) surfaces using anisotropic etching. This process is applicable for single crystal silicon, but not for mc-Si, which exhibits different crystallographic orientations, resulting in not only non-uniform texturing but also small steps between grains of different orientation.

Several promising methods are being explored for texturing mc-Si including RIE texturing, porous Si texturing, acidic isotropic etching, and mechanical V-grooving. Mechanical V-grooving has evolved from a single to multi-blade, high throughput process and has resulted in very low surface reflection and a $\sim 1\%$ enhancement in cell efficiency. A process based on SP of 100 cm^2 mc-cells and firing through SiN_x was adapted to the processing of mechanically grooved structures and resulted in 16.6% efficiencies [14]. However, additional work is required to assess the reproducibility of SP contacts on such deep V-grooved cells.

RIE texturing involves immersing bare silicon wafers in a direct chlorine plasma [15]. By controlling the gas flow and process conditions, homogeneous microscopic pyramid-like structures are formed independent of the crystallographic orientation of the wafer. However, such surfaces increase surface recombination velocity. A short wet chemical etching improves the surface quality but at the expense of surface reflectance. Inomata et al. produced a 17.1% efficient 225 cm^2 mc-Si cell using RIE texturing with Cl_2 gas, emitter diffusion from POCl_3 , PECVD SiN_x bulk and surface passivation, and contacts formed by evaporation and lift-off photolithography [16]. This result suggests that RIE surface texturing can be done without causing performance degradation.

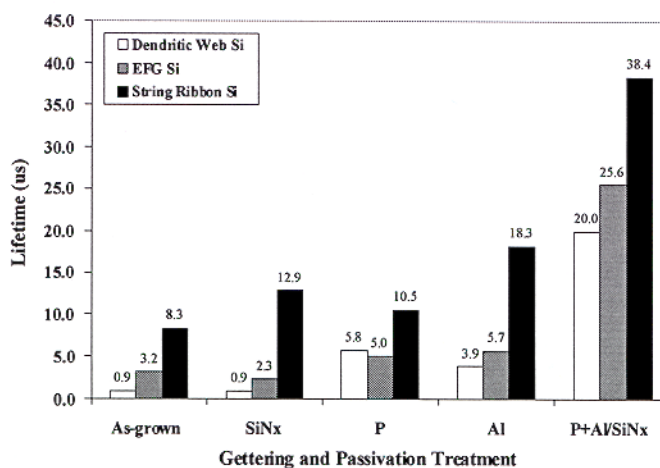
Another promising texturing technology involves the formation of a porous Si layer by short acidic etching in a solution of HF and nitric acid. By adjusting the solution composition and processing conditions, one can change the porosity, refractive index, and antireflection properties. Porous Si also shows diffused transmission and thus serves the purpose of light trapping. Porous Si layers with only 5.5% optical loss (reflection and absorption) have been achieved [17], which is superior to single layer SiN_x and TiO_2 coating. Surface passivation seems to be the weak point because of which, the short wavelength response of the PS cells is low. Laboratory cell efficiencies of 14.3% have been achieved on monocrystalline Si with SP contacts [17]. When a PS layer is formed after the front contact, one obtains essentially a selective emitter. However, the high surface recombination velocity negates the beneficial effect of a selective emitter.

Recently another simple, low-cost technique based on isotropic etching using acidic solutions has been developed at IMEC [18]. Large area ($12.5\text{ cm} \times 12.5\text{ cm}$) SP mc-Si cells fabricated with this surface texturing process produced a 15.7% efficiency. The process sequence involved iso-texturing, POCl_3 emitter, PECVD SiN_x , SP front and back metallization and co-firing. The proprietary acid solution consists of a mixture of HF, HNO_3 , and some additives. The removal of saw damage is part of the texture etching which requires only one step to create texture from as-cut wafers.

2.2.6 Manufacturable Gettering and Passivation Techniques for Lifetime Enhancement

Model calculations in Figure 1 show that lifetime enhancement from 10 to 20 μs can give $\sim 0.9\%$ increase in efficiency for this cell design. Beyond 20 μs , there is only little to be gained from further increases in lifetime especially for a 100 μm thick device. Georgia Tech has shown a rapid, manufacturable process in a belt furnace using a PECVD SiN_x AR coating, can increase the bulk lifetime in most mc-Si beyond 20 μs (Figure 4) [19]. This process involves a 925-935°C/6 minute spin-on or SP phosphorus diffusion and gettering in the belt, followed by SiN_x deposition on the front, and SP Al on the back and a short 850°C/2 minute anneal in the belt furnace. The simultaneous anneal in the presence of Al enhances the SiN_x -induced hydrogenation of bulk defects and also achieves Al gettering.

Remote plasma hydrogen passivation (RPHP) has been shown to improve the efficiency of solar cells on low-quality and high-quality mc-Si by 0.4-1.7% (absolute) on average. The advantage of RPHP is that hydrogenation is performed without plasma induced surface damage associated with direct PECVD deposition of silicon nitride. Currently, best results have been achieved in 30-60 minute processes at 400°C [20].



3. Summary and Conclusions

This paper reviews the progress in mc-Si cell efficiencies and provides a roadmap for achieving $\geq 18\%$ mc-Si cells using low-cost materials and potentially low-cost cell fabrication technologies. In addition to reviewing some of the highest efficiency mc-Si cells, recent advances in promising and emerging technologies are discussed. Particular emphasis is placed on efficiency enhancing low-cost technologies such as back surface fields, defect gettering and passivation in a belt furnace, improved screen-printing, surface texturing, and selective emitters. Even though significant progress has been made, considerable research and development is still required to transform current 300-400 μm thick, 12-14% industrial cells to 100 μm thick 18-20% efficient cells in the near future.

Acknowledgements

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Silicon Solar Cell Manufacturing

10 Years of Volume Growth and Cost Reduction

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Abstract

The last decade has brought growth and maturity to the field of silicon solar cell manufacturing. It has not brought significant technical innovation. Wafer size and volumes have increased, wafer thickness has decreased, and manufacturers focused on equipment, throughput, and yield. These changes have been accompanied by a priority on cost reduction and profitability. Many manufacturers have given up the will to undertake the risk that accompanies new processes. Some exceptions exist. Increased understanding of the complicated materials issues affecting performance has generated modest performance increases, but no breakthroughs in processing. Increasing the use of hydrogen for defect passivation and re-inventing the front contact represent significant areas for improvement.

The Business Environment

The annual growth rates of some of the larger manufacturers are shown in Figure 1. The increases are very large, reaching 100% increases per year for MW levels of production. The changes have also been very erratic.

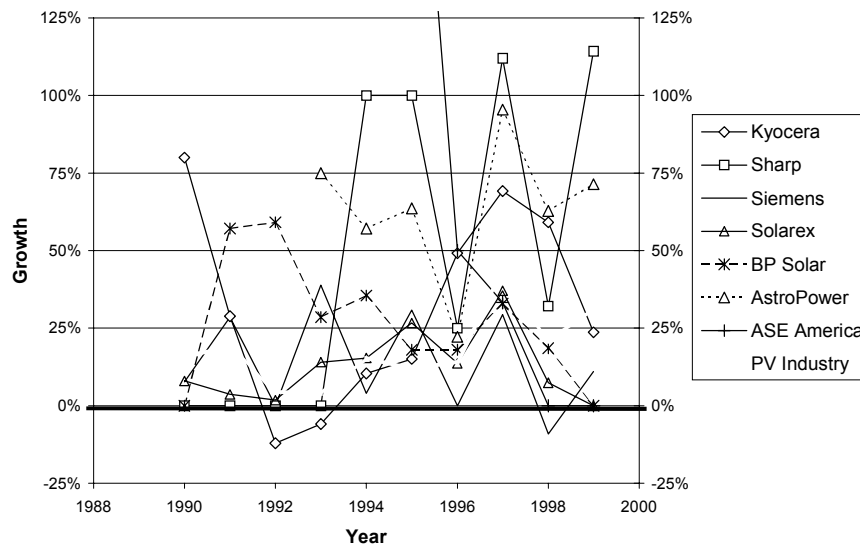


Figure 1. Annual growth rates of the some of the largest solar cell manufacturers. (From PV News, Paul Maycock Editor).

Process Development

No two solar cell manufacturers have the same process sequence, therefore summarizing the industry changes over the past ten years requires some gross generalizations. Table 1 shows the generic baseline process for single crystal and multicrystalline silicon wafers as practiced in 1990 and in 2000. Sheet processes, which have seen significant growth in this ten year period, avoid the wafering step altogether.

Table 1. The “generic” baseline process today and 10 years ago. Changes are shown in *italics*.

	1990 Baseline Process	2000 Baseline Process
Wafering	<i>ID Saws</i>	<i>Wire Saws</i>
Damage Etch	NaOH Batch Etching	NaOH Batch Etching
Bulk Gettering		
Diffusion	<i>Tube</i> Phosphorus Diffusion	<i>Belt</i> Phosphorus Diffusion
Phos Glass Etch	HF Batch Etching	HF Batch Etching
AR Coating	APCVD	APCVD
Back Surface Field		<i>Al ink or B diffusion</i>
Metal Contacts	2 Step Screen Print	2 Step Screen Print

A generally improved understanding of impurities and defects in silicon has brought into question every thermal treatment used in the solar cell process. Optimization of specific thermal schedules has significantly effected performance, without requiring equipment changes. The general trend in heat treatments has been to move away from long, slow, batch processes and towards high speed “rapid thermal processing”-like sequences. This has been the case for contact firing for some time and the diffusion process has evolved along those directions over the past ten years. Manufacturers have historically been loath to discuss specific process information on this topic.

One of the biggest changes is the incorporation of a back surface field (BSF) into the print/fire contact sequence. This change has had a significant impact on performance with little extra processing cost. As lifetimes have increased through better materials and thermal processing, and wafers have become thinner, the diffusion lengths have drawn close to the wafer thickness. The incorporation of a BSF limits back surface recombination, increasing current and voltage. Gettering may be occurring during this process, but is being treated as a bonus, with little optimization being devoted specifically to this effect.

Hydrogenation has been researched and reviewed at great length in the past ten years. The beneficial effects for bulk passivation has been proven, but the lack of a low-cost, high-throughput process has limited its wide-spread use. The development of a silicon nitride antireflection coating process that includes hydrogen passivation has gained some

acceptance in the industry. Equipment availability, cost, and throughput issues are still present.

In terms of overall device performance, the existing front contact technology – a heavily doped emitter with screen printed contacts – is the largest performance compromise for manufacturing concerns. The buried contact process has been shown to recapture those losses, but has not yet gained wide-spread acceptance. Selective emitters hold great promise, however only prototype laboratory processes exist today. This remains an area for significant potential improvement.

Characterization has matured from slow single wafer studies to fast in-line process monitoring, resulting in significant yield improvements. The development of manufacturing friendly lifetime measurements in the past 10 years has had an important impact.

Summary

While solar cell performance has remained an important issue for manufacturers in the past decade, yield and throughput have demanded equal or more attention.

The materials work that has been reported at this conference over the past decade has established a scientific background that has helped drive process optimization, but has not yet prompted a new generation of processes. Industry solar cell performance continue to lag behind laboratory efficiency records and the detailed understanding of why those differences exist – at a material level – will help close the gap in the near future. There is important materials and process work yet to do for silicon solar cells.

DEFECTS IN SILICON AND THEIR ELECTRONIC PROPERTIES

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Defects in silicon can be grouped into four categories using dimensionality as a criterion: zero-, one-, two-, and three-dimensional. The respective examples are point defects, dislocations, stacking faults, and precipitates. In the following, we consider the description of these defects, and their electronic properties.

DESCRIPTION OF VARIOUS DEFECTS

Zero-Dimensional Defects – This category includes vacancies, interstitials, vacancy-interstitial pairs, dopant atoms intentionally added to control the conductivity of silicon, and impurities that are unintentionally incorporated as contaminants during material growth and processing.

Silicon crystallizes in the diamond-cubic structure. Figure 1 shows this structure in which one of the tetrahedrally coordinated silicon atoms has been removed. The resulting defect is called a Schottky vacancy. The formation of a vacancy results in four dangling bonds that, as discussed later, impart electrical

properties to those defects. The lattice must also relax around the vacancy. The energies of formation and migration for Schottky vacancies in silicon are, respectively, ~2.3 and 0.18 eV.

The concentration of vacancies (n) in silicon at a given temperature can be determined from the following expression:

$$n = n_o \exp\left(\frac{-E_D}{kT}\right),$$

where n_o is the total number of atoms/volume, E_D is the energy of formation of a vacancy, k is the Boltzmann constant and T is the temperature.

A Schottky interstitial is the second elementary point defect that can exist in silicon. Figure 2 shows the positions of some of the interstitial sites in the diamond-cubic structure. An interstitial defect can be formed by inserting a silicon atom into one of the holes in the structure. The energy of formation of interstitials in the loosely packed diamond-cubic structure is low in comparison to those in the close-packed structures because the distortions associated with the interstitials in these structures are considerably larger than that in the diamond-cubic structure. A value of 1.1 eV is often associated with this type of defect in silicon. Frenkel defects, i.e., vacancy-interstitial pairs can also form.

Impurities in the form of dopants are added to silicon to control its carrier concentration and type of conductivity. These impurities replace host atoms located on lattice sites, and therefore are referred to as substitutional impurities. Since sizes of the substitutional impurity and the host atom are likely to be different, strains are introduced into the lattice during the impurity

incorporation. The strain issue can be addressed by referring to Table 1 that shows tetrahedral covalent radii of various atoms.

The tetrahedral radius of the atom r_A of a host lattice can be correlated with that of a dopant impurity r_B via the following expression:

$$r_B = r_A (1 \pm \delta),$$

where δ is referred to as the misfit factor. The misfit factors for commonly used dopants in silicon are listed in Table 2. The misfit factors provide a measure of the strain introduced into the crystal due to the incorporation of the dopants: the larger the misfit factor, the larger the strain.

One-Dimensional Defects – Dislocations are one-dimensional defects and represent boundaries between slipped and unslipped regions of a crystal. In silicon they glide on $\{111\}$ planes and their Burgers vector is $\frac{a}{2} \langle 110 \rangle$, where a is the lattice parameter. A combination of a slip plane and a Burgers vector is called a slip system. There are twelve such systems in silicon, and they are schematically shown in Figure 3. The Peierls, i.e., the stress required at 0K to move a dislocation from one equilibrium position to the next, is fairly high in silicon, and the Peierls valleys are aligned parallel to $\langle 110 \rangle$ directions lying in the $\{111\}$ plane. As a result, dislocations observed in silicon deformed at low and moderate temperatures tend to lie along $\langle 110 \rangle$ and are of 60° type, i.e., the angle between the line direction and the Burgers vector is 60° .

Two types of $\frac{a}{2} \langle 110 \rangle$ perfect dislocations can form in silicon. Referring to Fig. 4 that shows a projection of the diamond-cubic structure onto a (110)

plane, a 60° dislocation can be produced by removing the material enclosed by surfaces 15, 56, and 64 and subsequently welding the surfaces 15 and 64. The extra half-plane of the resulting dislocation terminates between the narrowly spaced $(\bar{1}11)$ planes, and the dislocation belongs to the “glide set.” On the other hand, when the material is removed along the, 12, 23, and 34 surfaces and the surfaces 12 and 34 are welded together, the resulting imperfection is called a “shuffle set” dislocation, and its extra half-plane terminates between the widely separated $(\bar{1}11)$ planes.

Figure 5 shows three-dimensional perspectives of the 60° glide- and shuffle-set dislocations. Their most important feature is the presence of dangling bonds along the dislocation cores. As discussed later, these dangling bonds impart electrical activity to the dislocation and can affect carrier concentration and mobility in silicon.

Perfect $\frac{a}{2}\langle 110 \rangle$ glide-set dislocations can dissociate into two $\frac{a}{2}\langle 112 \rangle$

Shockley partials. For example consider the case of $\frac{a}{2}\langle 1\bar{1}0 \rangle$ glide-set

dislocation moving on a (111) slip plane. This dislocation can dissociate according to the following reaction:

$$\frac{a}{2} [1\bar{1}0]_{(111)} \rightarrow \frac{a}{6} [2\bar{1}\bar{1}]_{(111)} + \frac{a}{6} [1\bar{2}1]_{(111)}$$

The schematic on Figure 6 illustrates this dissociation, which shows the projection of the diamond-cubic lattice on the (111) plane. On the

other hand, shuffle-set dislocations cannot dissociate into Shockley partials.

The orientations of Shockley partials resulting from dissociation depends on the orientation of the perfect dislocation. Thus, these partials can have various orientations. Figure 7(a) shows unreconstructed cores of 30° and 90° partials resulting from the dissociation of a 60° perfect dislocation. To further lower the energy, the cores can undergo reconstruction as illustrated in Figure 7(b) for a 30° partial.

Experimental observations indicate that dislocations in silicon are dissociated into Shockley partials and glide in the dissociated configuration. These results suggest that glide-set dislocations are primarily involved in the deformation behavior of silicon.

Two-Dimensional Defects – Stacking faults, twin boundaries, subboundaries, and grain boundaries are typical examples of two-dimensional defects. We first consider the formation of stacking faults and twins, followed by a brief introduction to the structure of subboundaries and grain boundaries.

Stacking faults and twins. Stacking faults in silicon form on $\{111\}$ planes in two distinct ways: (1) by shear and (2) by the agglomeration of point defects. The schematic in Figure 8 illustrates the situations resulting from shear. Figure 8(a) shows the Aa Bb Cc Aa stacking of $\{111\}$ planes in silicon.

Now imagine a situation in which $\frac{a}{6} [\bar{1}21]$ displacement is imposed on some of the atoms in the A-a layers that move as a pair. As a result, the atoms below the

doubled dashed line would move into the B-b position as shown in Figure 8(b).

The imposition of the $\frac{a}{6} [\bar{1}\bar{2}1]$ displacement on the A-a layers also causes the movements of layers below this pair as illustrated in Figure 8(b). The resulting arrangement constitutes an intrinsic stacking fault. Since faults terminating within a crystal must be bounded by partial dislocations, the position of an $\frac{a}{6} [\bar{1}\bar{2}1]$ Shockley dislocation that bounds the intrinsic fault in Figure 8(b) is shown in Figure 9.

If we examine the layer arrangement across the C-c pair that is dashed in Figure 8, we find that B-b pairs are present on either side of the C-c pair, see Figure 8b; i.e., the atomic arrangement is reflected across the C-c layer. In other words, an intrinsic fault is one double-layer thick twin. In the case of the diamond-cubic structure, the "true" mirror symmetry exists across the C-c pair. Furthermore, unlike the case of $\frac{a}{2} [1\bar{1}0]$ dislocations, the formation of an intrinsic stacking fault does not produce dangling bonds at the fault surface.

An extrinsic stacking fault can be formed by imposing a second $\frac{a}{6} [\bar{1}\bar{2}1]$ displacement on the C-c pair that lies below the first shear plane. The resulting layer arrangement for an extrinsic fault is shown in Figure 8c. An examination of Figure 8 would reveal that the fault is a two double-layer thick twin. Likewise, a three-layer-pair thick twin can be produced as the schematic in Figure 8d shows.

Now consider a situation where vacancy discs form on the A-a planes, as shown in Figure 10a. This arrangement is unstable, and to eliminate it, the adjoining plane pairs C-c and B-b collapse around the hole, resulting in an intrinsic stacking fault as illustrated in figure 10b. Since the displacement associated with the collapse is along $[\bar{1}\bar{1}\bar{1}]$ direction, the Burgers vector of the partial bounding the fault is $\frac{a}{3}[\bar{1}\bar{1}\bar{1}]$ and is called a Frank partial. Furthermore, the layer arrangements in Figures 9b and 10b are identical within the faulted regions. However, the approaches used to achieve these configurations are different. In Figure 8b, some of the atoms in the A-a layers have been displaced into the B-b positions, whereas they have been removed in Figure 10b.

The formation of extrinsic faults resulting from the agglomeration of interstitials can be discussed in a similar manner. The schematic in Figure 10c shows the final-layer arrangement within the faulted region and the bounding partial. This arrangement is identical to that shown in Figure 8c, but it has been achieved via a different route, as discussed in the case of an intrinsic fault. Since the fault formation involves an insertion of a B-b plane-pair, the adjoining pair would have to be displaced outwards as shown in Figure 10c. Again, a Frank partial bounds the fault, but now its Burgers vector is a $\frac{a}{3}[111]$.

The preceding discussion shows that the conditions required for the formation of faults by shear and from agglomeration of point defects are different. In the case of shear faults, stresses must exist in the material to move Shockley partials to expand the faulted regions. These stresses could develop

during the growth of bulk crystals and epitaxial layers. On the other hand, the agglomeration case requires nonequilibrium concentrations of point defects. Again, appropriate conditions could evolve during the growth of bulk crystals, oxidations of silicon, diffusion, and ion implantation.

Subgrain boundaries and grain boundaries. State-of-the-art silicon crystals are highly perfect. As a result, different regions of crystals are not misoriented from each other. However, this is not true in the case of III-V and II-VI compound semiconductor crystals: Misorientations exist between cellular regions present in as-grown crystals. Polycrystalline silicon is also being used as emitters and gate contact in bipolar and metal-oxide-semiconductor transistors.

Depending on the misorientation between the adjoining crystals, the resulting interfaces are termed subgrain boundaries and grain boundaries. *Subgrain boundaries* separate regions that are misoriented by a very small amount, say 0 to 5°, whereas *grain boundaries* delineate interfaces between highly misoriented regions. An important question is, How can we describe these interfaces in terms of dislocations?

The subgrain boundaries are of three types: tilt, twist, and mixed. Consider a situation where a grain can be brought into the same orientation as another grain by a rotation around an axis. If the rotation angle is small and the rotation axis lies in the boundary, the subgrain boundary is a tilt boundary. On the other hand, if the rotation axis is perpendicular to the boundary, it is a pure

twist boundary. In general a boundary is of a mixed character, containing both tilt and twist components.

A formalism has been developed that describes subgrain boundaries in terms of dislocations. A symmetrical tilt boundary between two grains will consist of edge dislocations. If the tilt angle is θ and the Burgers vector of the dislocations is b , then separation (D) between the dislocations is given by the following expression:

$$D \cong \frac{b}{\theta}$$

The above equation shows that as the misorientation angle θ between the two grains increases, the separation between dislocations defining a subgrain boundary decreases.

The elegant work on subboundaries in Ge crystals proved that tilt boundaries can be described in terms of dislocations. Figure 11a shows an example of a subboundary in Ge. Figure 11a shows a row of etch pits observed at a subboundary between two Ge crystals, and Figure 11b shows a diagrammatic representation of the observed arrangement of dislocations, revealed by etch pits. Small-angle, pure-twist boundaries can also be interpreted in terms of networks of screw dislocations that lie in the boundary. Again, the separation between dislocations within the network varies with the angle of misorientation: the larger the angle, the smaller the separation between the screw dislocations.

The energy E per unit area of a low-angle boundary is given by an expression

$$E = E_0 \theta (A - \ln \theta),$$

where constant E_0 is a function of the elastic properties of a material and A is a constant that depends on the core energy of an individual dislocation. As the misorientation angle increases, the dislocation spacing decreases, leading to core overlap. As a consequence, the distortion near a dislocation no longer corresponds to that of an isolated dislocation. Under these conditions, the description of grain boundaries in terms of isolated dislocations has little physical significance. An alternative approach is based on the concepts of the coincident-site lattice and the displacement-shift complete lattice. Grain boundaries are modeled in terms of arrays of dislocations belonging to the coincident-site lattice, and local deviations in misorientation between the two grains are described in terms of dislocations belonging to the displacement-shift complete lattice.

Three-Dimensional Defects

Precipitates and inclusions constitute three-dimensional defects. Such defects could form during the growth of doped crystals when the solid solubility limit of a dopant is exceeded and also during processing of semiconductors. Precipitates can exist in three forms: coherent, partially coherent, and noncoherent. If a precipitate has the same crystal structure and a lattice parameter similar to that of the matrix, the precipitate can form low-energy coherent interfaces with the matrix on all sides as shown in Figure 12a. This type of coherency requires the respective lattices to have orientation relationships. However, coherency can still be maintained at the precipitate-matrix interface even when the precipitate

volume is slightly different from that of the matrix consumed in its formation. This situation is shown in Figure 12b when the precipitate volume is smaller than that of the matrix consumed. Generally, to produce a coherent matrix-precipitate interface, both lattices are distorted, as illustrated in Figure 12b. Based on the interface energy considerations, it is favorable for a precipitate to be surrounded by low-energy coherent interfaces. However, this condition is not generally feasible when the precipitate and the matrix have different crystal structures. For certain situations there may be a plane that is more or less identical in each phase, and by choosing the correct orientation relationship, a low-energy coherent interface can be formed. However, along other planes of the precipitate, matching with the matrix is poor, resulting in high-energy incoherent interfaces that can be described in terms of dislocations. On the other hand, when the two phases have completely different crystal structures or when the two lattices have a random orientation relationship, the formation of coherent or partially coherent interfaces is not possible. In this case, the matrix-precipitate interfaces are noncoherent, and the precipitate is said to be "incoherent." This situation is shown schematically in Figure 12c. Except in the case of perfect coherency shown in Figure 12a, the coherency strains exist at the coherent and partially coherent interfaces. Furthermore, the noncoherent interfaces are defined by interfacial dislocations.

ELECTRONIC PROPERTIES OF DEFECTS

The formation of defects in semiconductors creates a local electronic disturbance because of the nature of the atomic bonding. The complexity of the

disturbance depends on the dimensionality of the defects and the type of semiconductor. Plausible situations that arise in silicon are discussed next.

Zero-Dimensional Defects

When a vacancy is formed in the diamond-cubic structure of an elemental semiconductor (see Figure 1), each atom constituting a tetrahedron has an unpaired electron. Consequently, there is a tendency for the pairing of these unpaired electrons. As a result, vacancies tend to exhibit acceptor like behavior. In principle, a distinct energy level within the band gap should be associated with each pairing, and each energy level must occur at a progressively higher energy because of the electrostatic interactions between the captured electrons.

Consequently, a vacancy in silicon can give rise to four distinct energy levels in the band gap. Experimentally, the acceptor levels at 0.11 and 0.4 eV from the conduction-band edge have been identified in silicon by a number of investigators. In addition, a donor level at 0.35 eV from the valance-band edge has also been observed and is attributed to bond distortion that must occur in the vicinity of a vacancy.

The situation regarding interstitials can be addressed in a similar manner. An interstitial has four valence electrons that are not involved in covalent bonding with the adjoining atoms. The successive loss of these unpaired electrons to the conduction band could, in principle, result in four different donor levels within the band gap. Experimentally, a singly ionized donor level at 0.91 eV below the conduction band edge is seen in silicon. The energy levels associated with point defects in silicon are also fairly deep. They serve as

centers for minority carrier recombination and thus cause a decrease in the carrier lifetime. This decrease is inversely proportional to the concentration of point defects.

One-Dimensional Defects

The introduction of dislocations in covalently bonded semiconductors produces two important effects. First, as a result of the elastic distortions associated with a dislocation, band bending occurs in its vicinity. Second, dangling bonds are created along the core of the dislocation.

Many models have been proposed to rationalize the electronic properties of dislocations. One of the models assumes that dislocation states can be represented by a one-dimensional band that is empty when the dislocation is in the neutral state. This model cannot account for the observed reduction of the hole density in p-type germanium after deformation. To rationalize this behavior, it is envisaged that the dislocation band is half filled in the neutral state or that energy bands associated with screws and 60° dislocations are split and that dislocation kinks give rise to deep donor and acceptor levels, which are located between the dislocation levels. The latter two models are depicted in Figure 13.

Based on the models shown in Figure 13, we can speculate on the electronic behavior of perfect dislocations in n- and p-type silicon. In an n-type material, donor impurities can provide electrons to fill either the half-filled band of a dislocation, see Figure 13a, or E_{DA} in Figure 13b; that is, the dislocation behaves as an acceptor. As a result of the acquisition of electrons, the

dislocation becomes negatively charged. The ramification is that the majority carriers will be repelled from the conduction-band states in a region contiguous to the dislocation. In addition, the positively charged donor impurities could be attracted to the dislocation to preserve the space-charge neutrality. This behavior leads to a space-charge region in the form of a cylinder in which positively charged donor ions surround the negatively charged dislocation. On the other hand, in a p-type material dopant atoms accept electrons from either a partially filled band or E_{DD} . Thus, dislocation behaves as a donor. The space-charge region is also formed in this case and consists of a positively charged dislocation surrounded by negatively charged acceptor ions.

Two-Dimensional Defects

Since faulted and unfaulted regions are coherently bonded to each other, dangling bonds are not created at the fault surface. Therefore, the surfaces of intrinsic and extrinsic faults and coherent twin boundaries in elemental as well as in compound semiconductors should not be electrically active. On the other hand, partials bounding various faults should be electrically active because of the presence of dangling bonds along the dislocation core. Furthermore, the electrical activity will vary with the orientation and character of the bounding partials. Also, the occurrence of reconstruction at the core may further affect the electrical activity.

As discussed earlier, we can treat subboundaries and grain boundaries as an assemblage of dislocations whose Burgers vector, orientation, and density depend on the crystallography of the boundary. Therefore, the electrical

activities of grain boundaries can be analyzed in terms of the electrical behavior of dislocations constituting a boundary.

Three-Dimensional Defects

In the case of semicoherent and noncoherent precipitates, dislocations are present at the matrix-precipitate interface. These dislocations can impart electrical activity to these interfaces. Thus, the influence of the semicoherent and noncoherent precipitates on the electronic properties of semiconductors can also be analyzed in terms of the electronic behavior of dislocations constituting the matrix-precipitate interface.

In summary, a formalism has been developed to describe various types of defects that could occur in silicon. The influence of these defects on electronic properties is also considered.

FURTHER READING

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TABLE 1

Tetrahedral covalent radii of different atoms in nm

	Be	B	C	N	O	F
	0.106	0.088	0.077	0.070	0.066	0.064
	Mg	Al	Si	P	S	Cl
	0.14	0.126	0.117	0.110	0.104	0.099
Cu	Zn	Ga	Ge	As	Se	Br
0.135	0.131	0.126	0.122	0.118	0.114	0.111
Ag	Cd	In	Sn	Sb	Te	I
0.152	0.148	0.144	0.140	0.136	0.132	0.128
	Hg					
	0.148					

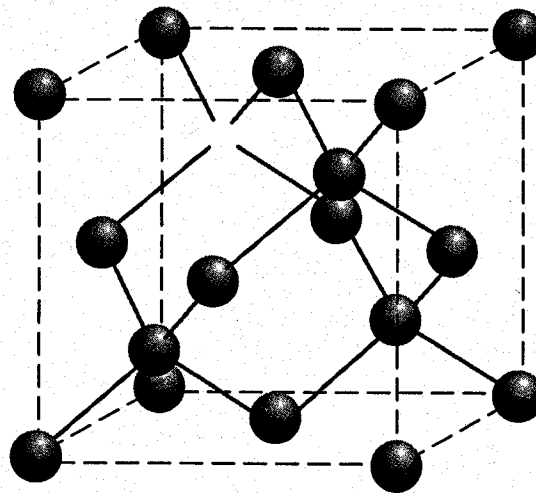
According to Pauling (1960).

TABLE 2

Misfit factors of commonly used dopants in silicon

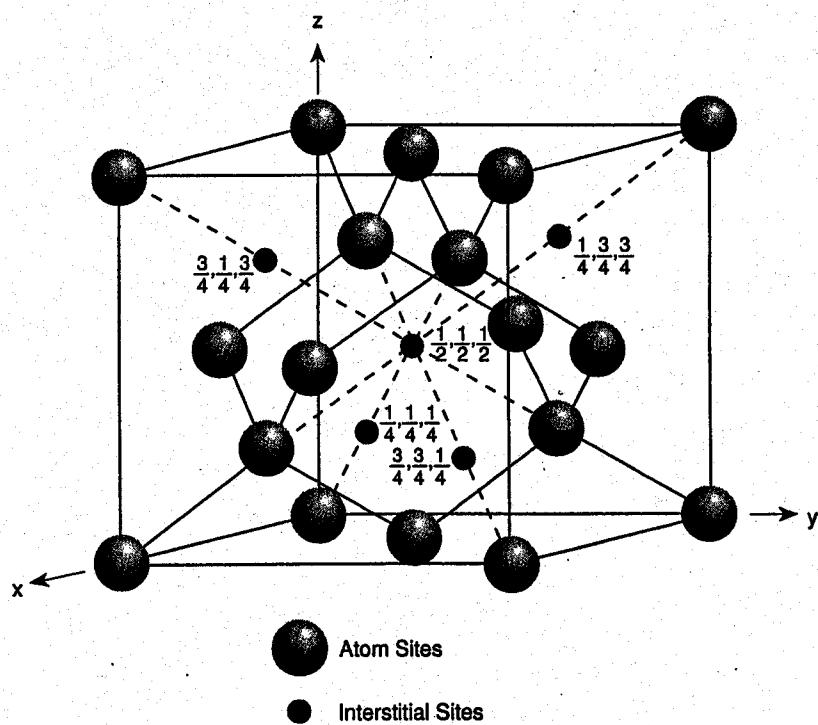
n-type			p-type		
P	As	Sb	B	Ga	Al
0.068	0	0.153	0.254	0.068	0.068

FIGURE 1



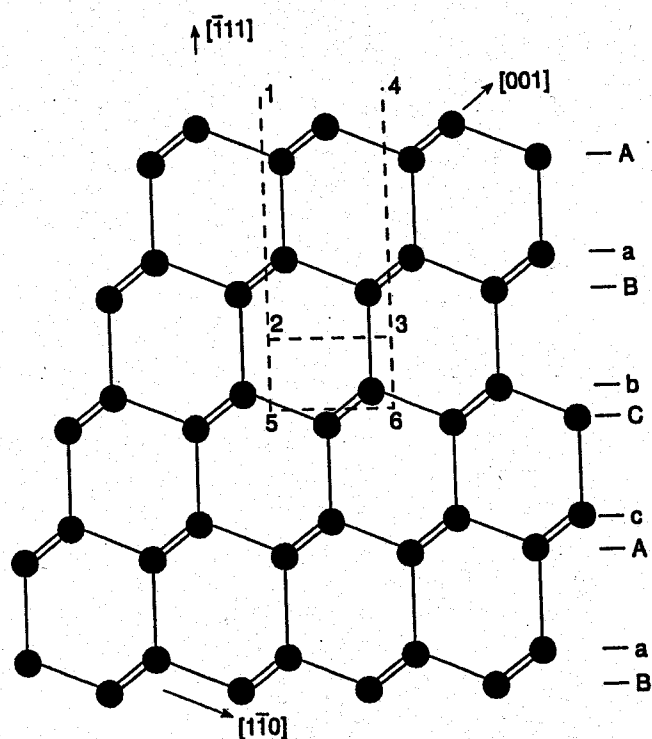
A vacancy in the diamond-cubic structure. Note that four unsaturated bonds, that is, dangling bonds, are present around the vacancy. The lattice must also relax around the vacant site.

FIGURE 2



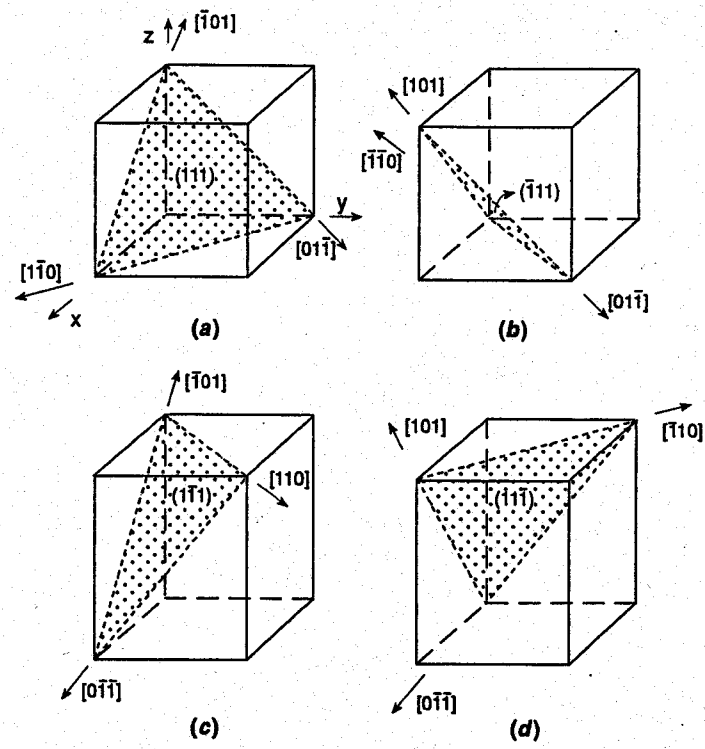
Some of the interstitial sites in the diamond-cubic structure.

FIGURE 3



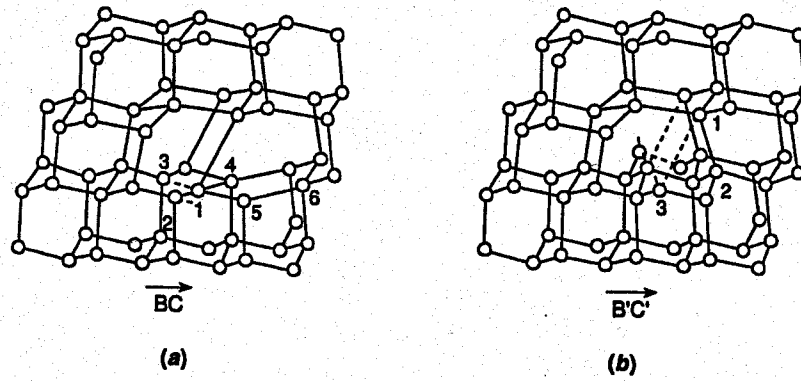
Diamond-cubic lattice projected onto a (110) plane. The $(\bar{1}11)$ planes are perpendicular to the plane of the paper and appear as horizontal lines. A dislocation belonging to the glide set can be formed by removing the material enclosed by surfaces 15, 56, and 64 and then welding the 15 and 64 surfaces; whereas a shuffle-set dislocation can be formed by removing the material along the 12, 23, and 34 surfaces and subsequently welding the 12 and 34 surfaces.

FIGURE 4



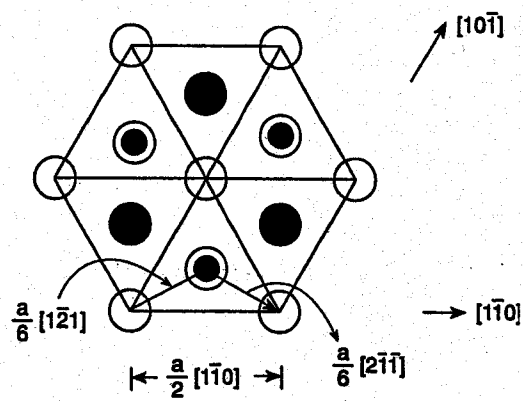
Schematic showing various slip systems in the diamond-cubic and zinc-blende structures.

FIGURE 5



Possible three-dimensional projections of (a) a 60° glide-set dislocation and (b) a 60° shuffle-set dislocation. Note the presence of dangling bonds along dislocation cores in both cases. (After Hirth and Lothe [1982].)

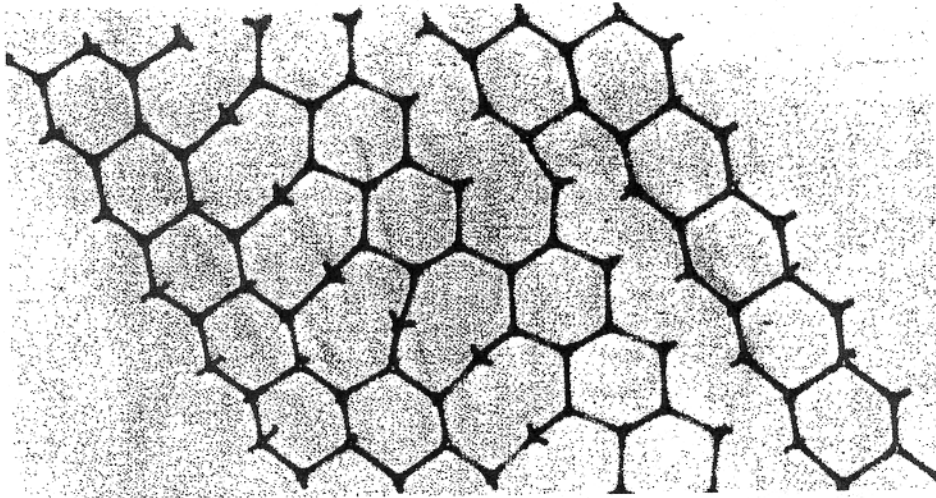
FIGURE 6



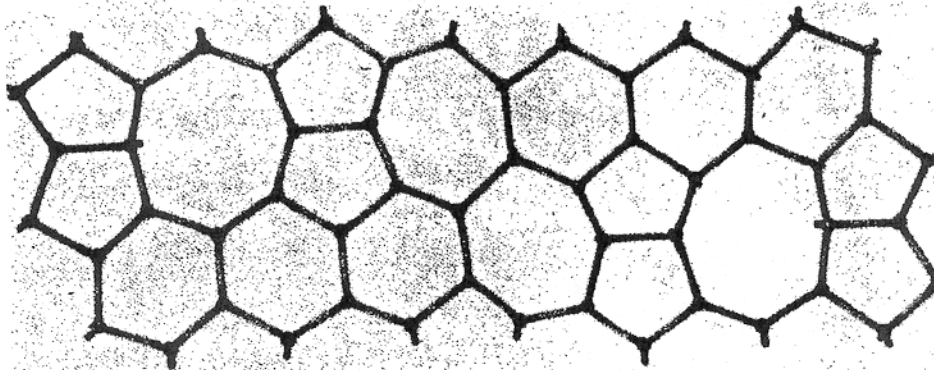
Schematic illustrating the projection of the diamond-cubic structure on a (111) plane.

- Projection of Atoms in A and a Layers
- Projection of Atoms in B and b Layers
- Projection of Atoms in C and c Layers

FIGURE 7



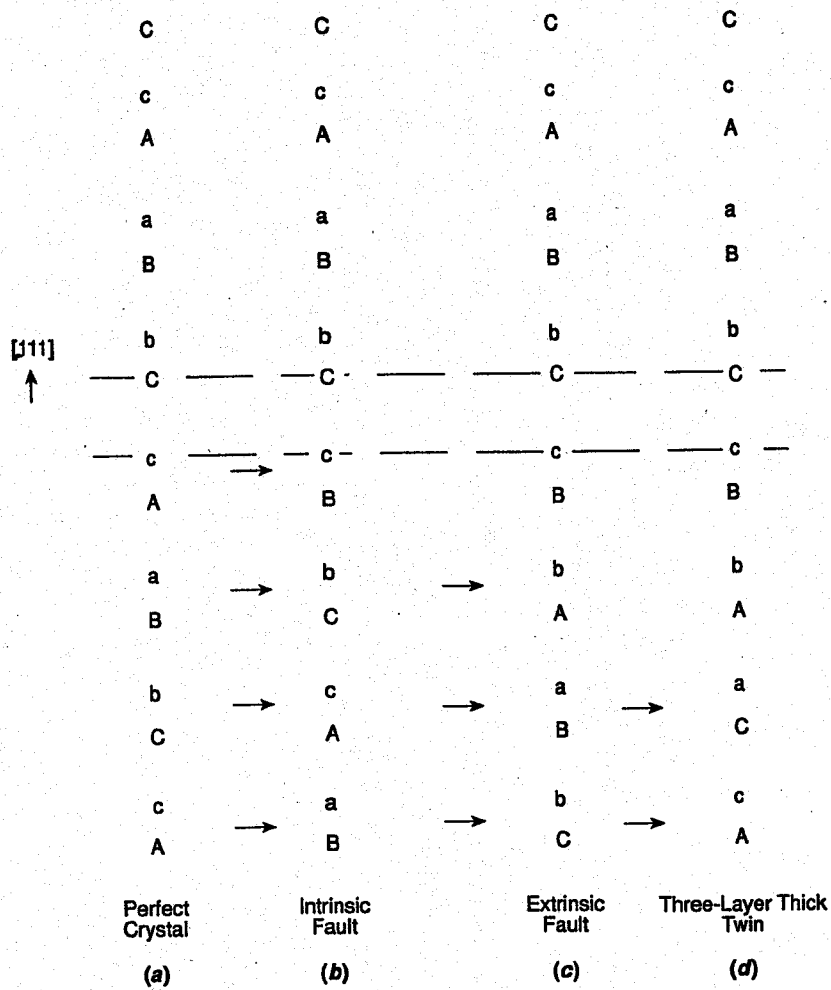
(a)



(b)

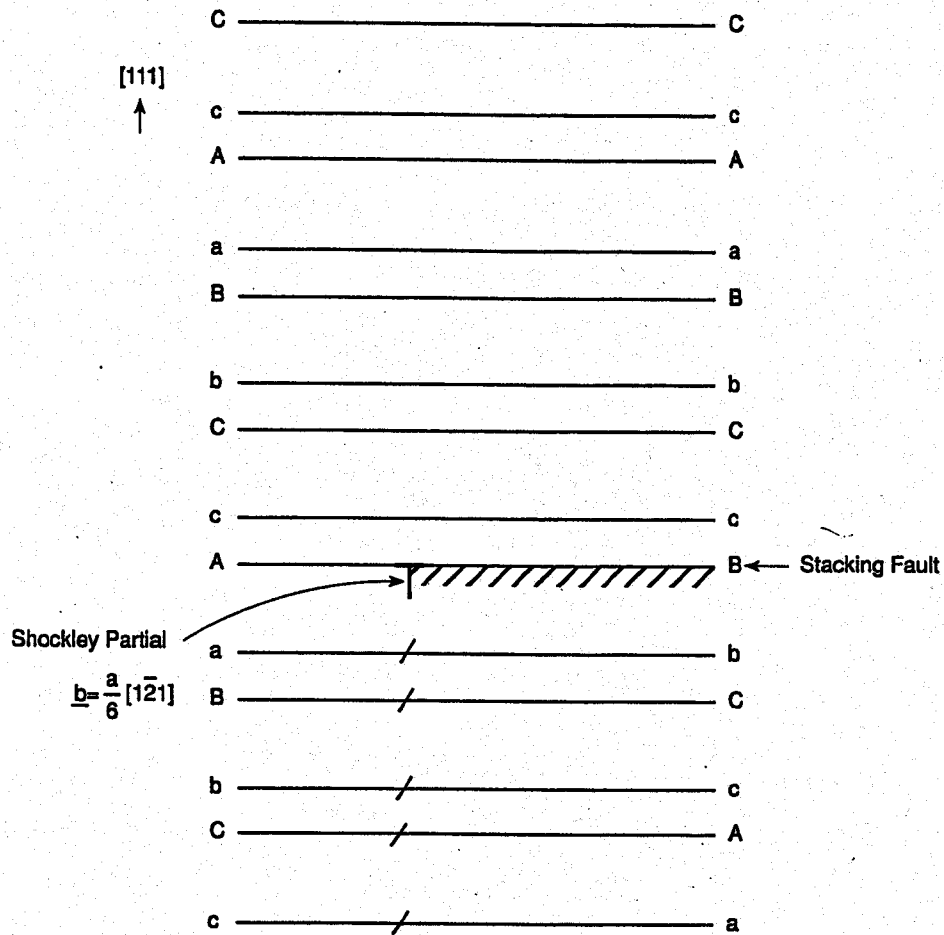
(a) Ball and stick model showing the dissociation of a 60° dislocation into a 30° Shockley partial (left) and a 90° partial (right); dislocation cores are unreconstructed. Kinks are shown on both partials. Viewed normal to the slip plane; only a layer of atoms above and below the slip plane are shown. (b) Reconstructed 30° partial with a kink. (After Hirsch [1981].)

FIGURE 8



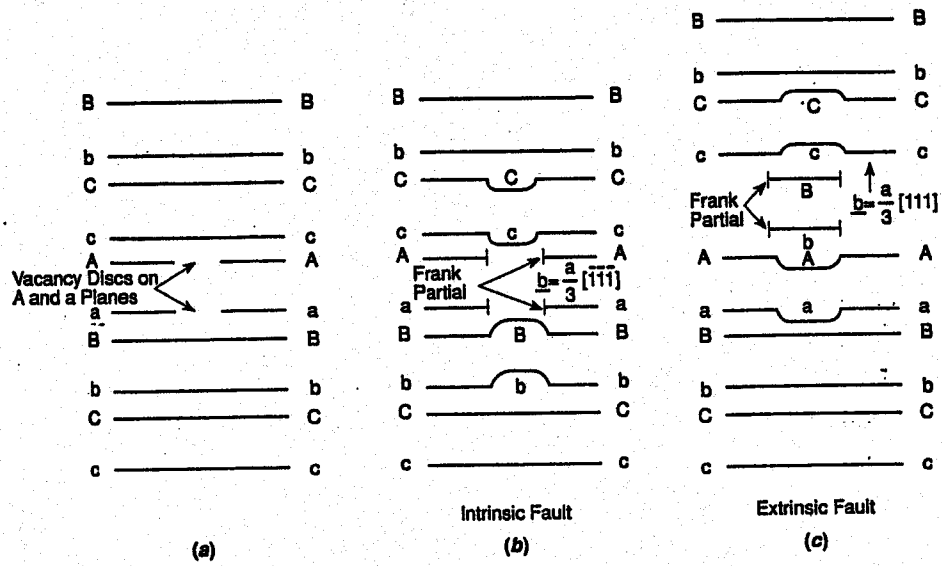
Schematic illustrating the formation of stacking faults and a three-layer twin in the diamond-cubic and zinc-blende structures by shearing of (111) planes: (a) perfect crystal, (b) intrinsic fault, (c) extrinsic fault, and (d) three-layer twin.

FIGURE 9



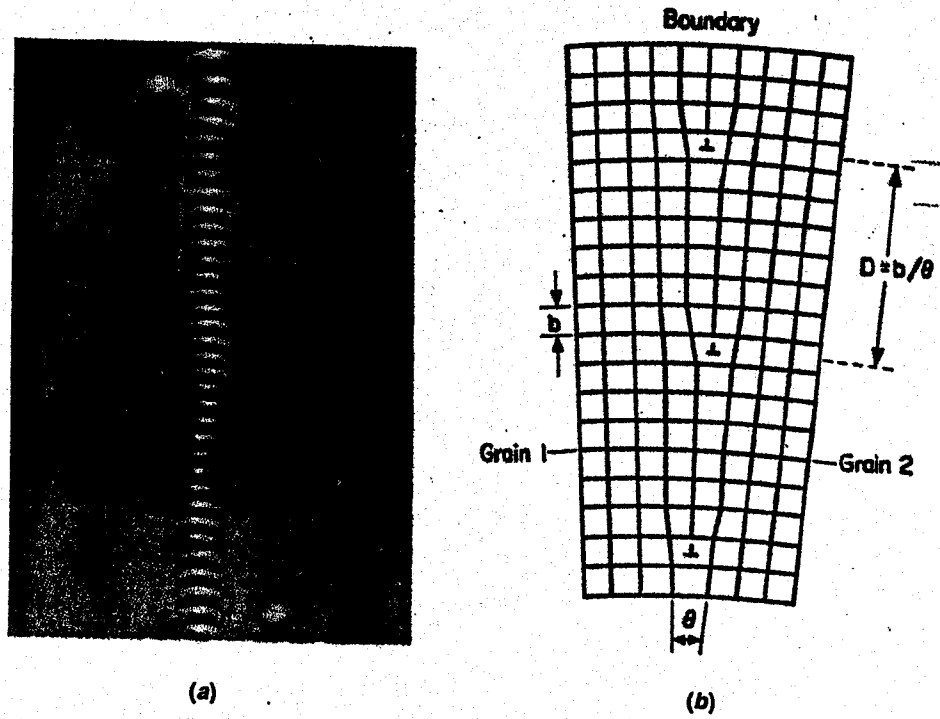
Schematic showing the position of the $a/6 [1\bar{2}1]$ Shockley partial that bounds an intrinsic stacking fault in the diamond-cubic and zinc-blende structures. The (111) planes are normal to the plane of the figure.

FIGURE 10



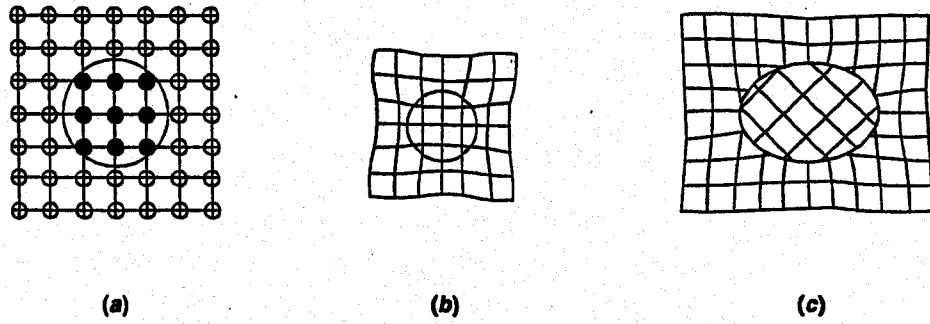
Schematics illustrating the formation of intrinsic and extrinsic stacking faults in the diamond-cubic and zinc-blende structures by the agglomeration of point defects on (111) planes: (a) layer arrangement after the formation of vacancy discs on the A-a plane pair, (b) intrinsic fault resulting from the collapse of the B-b and C-c pairs adjoining the vacancy discs, and (c) extrinsic fault resulting from the insertion of the B-b pair between the A-a and C-c plane pairs. A Frank partial bounds each fault, and the respective Burgers vectors are $a/3 [\bar{1}\bar{1}\bar{1}]$ and $a/3 [111]$.

FIGURE 11



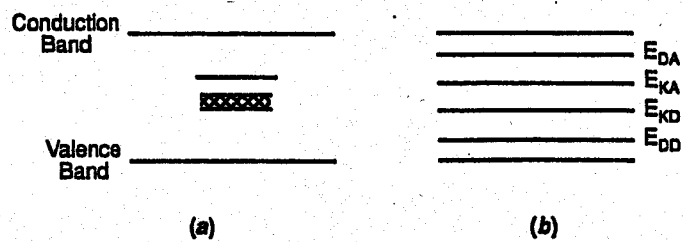
(a) A row of etch pits formed at the boundary between two Ge crystals. (b) Diagrammatic representation of the arrangement of dislocations revealed by the etch pits. (After Vogel *et al.* [1953].)

FIGURE 12



Schematics showing (a) a fully coherent precipitate associated with no strains, (b) a fully coherent precipitate associated with coherency strains, and (c) a fully noncoherent precipitate associated with misfit dislocations and strains.

FIGURE 13



Schematic of dislocation band models due to (a) Schröter and Labusch (1969) and (b) Hirsch (1979, 1981). E_{DA} , E_{KA} , E_{KD} and E_{DD} refer to acceptor and donor levels due to a dislocation and a kink, respectively. D and K stand for a dislocation and a kink.

Minority Carrier Recombination Properties of Metallic Precipitates in Silicon

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ABSTRACT

A quantitative model of the electrical activity of metallic precipitates in Si is presented. An emphasis is made on the properties of the Schottky junction at the precipitate-Si interface, as well as the carrier diffusion and drift in the Si space charge region. Carrier recombination rate is found to be primarily determined by the thermionic emission charge transport process across the Schottky junction rather than the surface recombination process. It is shown that the precipitates can have a very large minority carrier capture cross-section.

Metal and metal silicide precipitates can be prominent carrier recombination centers in Si. They are abundant in multicrystalline Si used for manufacturing of low cost solar cells. In order to evaluate the effect of impurities on solar cell performance, it is necessary to know the minority carrier capture cross-section of the impurity atoms as well as that of impurity precipitates. For most transition metals, the capture cross-section of individual atoms in solid solution in Si has been measured [1 - 3]. However, much less data is available regarding the electrical activity of metallic precipitates. It is known that such precipitates can act as very active recombination centers and significantly reduce minority carrier lifetime in semiconductors. They tend to form at crystal imperfections, dislocations and grain boundaries and in many cases are responsible for the recombination activity of such imperfections [4 - 9]. The electron beam induced current (EBIC) technique allows one to observe metallic precipitates in Si and measure their relative recombination activity. In EBIC experiments it was found that the recombination activity of metallic precipitates is very high [4, 6 - 8]. This can be explained by the presence of an electric charge on the precipitates due to Schottky effect [10 - 12]. Deep level transient spectroscopy (DLTS) study of metallic precipitates confirms this conjecture [13] and also indicates that precipitates form band-like states in the semiconductor bandgap [5, 13]. Also it was found that the recombination activity of precipitates decreases with the increase of the generation rate [14]. There have been several attempts to calculate the recombination activity of precipitates theoretically [15, 16], but they primarily focused on the formation of contrast in EBIC and did not attempt to predict the precipitate capture cross-section (CCS) based on its size and materials properties. Also, the issue of the recombination mechanism was not addressed. Understanding the mechanism of recombination at the precipitates and obtaining the associated CCS values are necessary to evaluate the effect of precipitated metallic impurities on the minority carrier lifetime. In this paper, we consider possible recombination mechanisms and present a model for calculating the precipitate CCS.

A metal or silicide precipitate forms a Schottky junction with Si, and therefore is charged and surrounded by a Si space charge region. When the semiconductor is illuminated, a generation of non-equilibrium carriers occurs, and their distribution is characterized by quasi Fermi levels,

separate for electrons and holes. In the absence of recombination at the precipitate these quasi Fermi levels are flat. This corresponds to a situation when there is an impermeable barrier at the precipitate-Si interface and no interface states. In the opposite situation, if the recombination at the precipitate-Si interface exists and is very (infinitely) fast, the equilibrium concentration of carriers is restored at the interface, and the quasi Fermi levels for electrons and holes merge (Fig 1a). Away from the interface, the positions of quasi Fermi levels are determined by the rate at which the carriers flow from the semiconductor bulk to the interface. This rate, in turn, is determined by the carrier diffusion and drift in the electric field, which is due to the charge on the precipitate and the space charge. In the absence of the electric field the concentration of minority carriers is much smaller than that of majority carriers everywhere in the semiconductor, and the supply of minority carriers is the limiting factor of the recombination process. If the electric field is present as described above, it attracts minority carriers to the precipitate and repulses majority carriers. Therefore, the supply of majority carriers is significantly decreased, whereas the supply of minority carriers is increased and may even exceed that of majority carriers. However, it cannot be qualitatively judged the supply of which type of carriers will be the limiting factor of the recombination process, and no a priori assumption should be made in that regard.

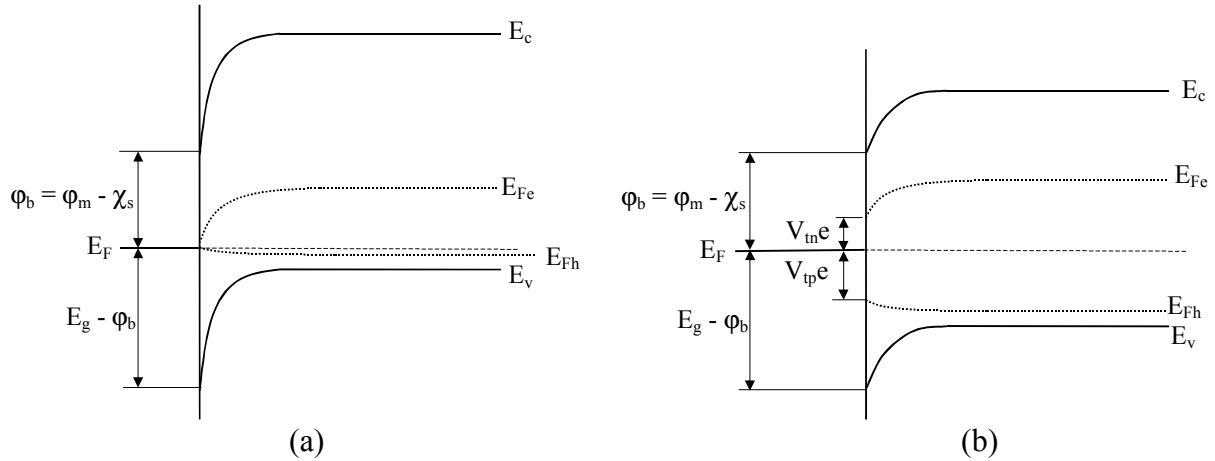


Fig. 1. Band structure of the precipitate with metallic properties in Si. (a) with infinite recombination rate at the interface; (b) with thermionic emission barrier for carrier transport at the interface.

Once the carriers reach the precipitate, they can recombine either in Si at the precipitate interface states or inside the precipitate. In the former case, the local carrier recombination rate is determined by the surface recombination velocity due to interface states, while in the latter case it is governed by the thermionic emission mechanism for charge transport across the Schottky junction. Regardless of the mechanism, the limited recombination rate will result in the quasi Fermi levels' not completely merging at the interface, but only approaching each other. Assume that there are no interface states at the precipitate. Electrons and holes still can flow through the precipitate-Si interface. Electrons entering the precipitate will have energies above the Fermi level in metal, but will rapidly attain Fermi-Dirac distribution. Similarly, holes entering the metal will create empty states below the Fermi level, which will be very rapidly populated by electrons. Thus, upon entering the precipitate, an electron-hole pair will almost immediately recombine. If there was no barrier for the charge carrier transport across the precipitate-Si interface, the

recombination rate would be sufficiently large, and the band diagram of the system would look like the one in Fig. 1a. However, the transport of carriers across the precipitate-Si interface gives rise to the thermionic emission potential at the interface. Generally, in the case of direct current across the Schottky junction, only the transport of majority carriers across the junction is involved, and the thermionic emission potential exists only for majority carriers. In the case of recombination current, there is transport of both types of carriers, and the thermionic emission potentials are essential for both majority and minority carriers (Fig. 1b). These potentials (V_m and V_{tp}) have opposite signs, and the ratio of their absolute values depends on the recombination current and effective masses of electrons and holes in the semiconductor. The existence of V_m and V_{tp} alters the charge on the precipitate, and hence, changes the position of the Fermi level in metal with respect to the semiconductor bands. At the surface of the precipitate, the carrier concentrations are determined by the Schottky barrier height ϕ_b , which is an intrinsic property of the material, and the thermionic emission potentials, which vary with the recombination current. Away from the precipitate surface, the carrier concentrations are controlled by diffusion, drift, generation, and background recombination due to centers other than precipitates, e.g. dissolved metal atoms.

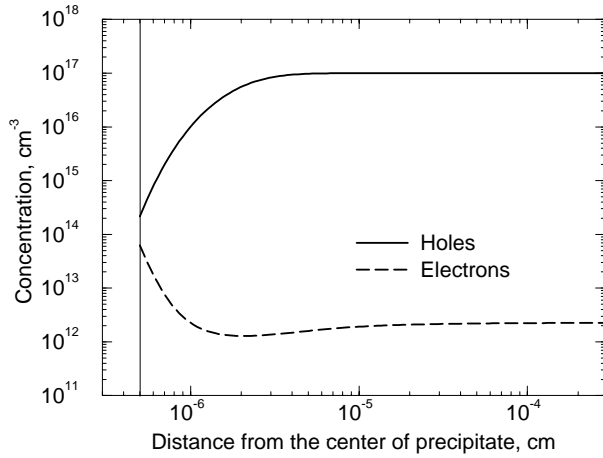


Fig. 2. Electron and hole concentration profiles around the precipitate. Parameters used: background recombination constant 10^5 s^{-1} , generation rate $10^{19} \text{ s}^{-1} \text{ cm}^{-3}$, precipitate concentration 10^{10} cm^{-3} , precipitate diameter 10^{-6} cm , p-type doping level 10^{17} cm^{-3} , $\phi_b = 0.68 \text{ eV}$ (FeSi)

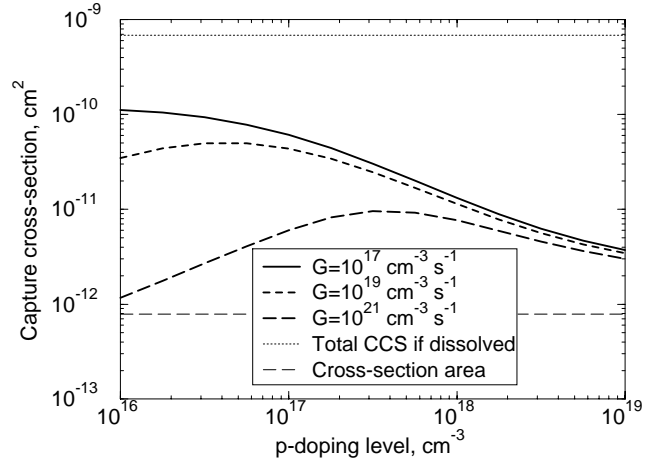


Fig. 3. Dependence of the precipitate capture cross-section on Si doping level at various generation rates. Other materials parameters used are the same as in Fig. 2.

To find out whether carrier recombination occurs primarily inside the precipitate or at the surface states, the interface recombination velocity of an ideal metal-semiconductor junction having no interface states was calculated based on the Schottky model. For p-type Si under the weak generation condition $n_0 \ll \delta n \ll p_0$, we obtain that the surface recombination velocity $s = Am_e^* T^2 / (emN_c) = 5.0 \times 10^{-6} \text{ cm/s}$ at room temperature [17]. Here A is the Richardson constant, m_e^* is the effective mass of an electron in Si, m is electron mass, T is the absolute temperature, e is the elementary charge, and N_c is the density of states in the conduction band. Since the interface recombination velocity due to interface states is usually much less than $5.0 \times 10^6 \text{ cm/s}$, it can be neglected. Furthermore, our modeling showed that even if the interface recombination velocity

due to interface states exceeds this value by a few orders of magnitude, the capture cross-section of the precipitate is affected only slightly.

The numerical modeling of recombination at precipitates was carried out using a variety of materials parameter values. Examples of electron and hole concentration profiles around the precipitate for p-type Si and FeSi precipitate are shown in Fig. 2. The CCS plots versus precipitate radius are shown in Figs. 3 and 4 along with the precipitate cross-section area, and the total CCS of dissolved metal atoms in Si of a number equal to that in the precipitate. The precipitate CCS is roughly proportional to its diameter, as predicted by the diffusion-limited model [18]. In most cases, the precipitate CCS value lies between its geometric cross-section area and the total CCS of its constituent metal atoms dissolved in Si. Under certain conditions, the precipitate CCS can even exceed the latter value. This is more characteristic of smaller precipitates. A higher precipitate concentration leads to a larger CCS. The model also predicts that the CCS drops at higher generation rates, as observed in experiments [14]. The dependence of CCS on ϕ_b and background recombination constant is relatively weak. Under the conditions considered, the supply of minority carriers is the limiting factor. The supply of holes becomes influential only at lower p-doping levels and higher generation rates, for which the weak generation condition no longer holds.

In order to verify the model, some available experimental data are fitted. The minority carrier diffusion length was calculated based on the published measured parameters for platelet-shaped NiSi_2 precipitates in n-type Si [12] using the model, Fig. 5. For each sample, two values of precipitate concentration were reported, as measured by TEM and EBIC, along with the precipitate dimensions. Accordingly, two values of minority carrier diffusion length were calculated and then compared to the experimental data. The generation rate and the background recombination constant were not known and were used as fitting parameters, $10^{18} \text{ s}^{-1} \text{ cm}^{-3}$ and 10^5 s^{-1} , correspondingly. The same fitting values were used for all samples. Variations of these values within an order of magnitude do not change the picture qualitatively. Other parameters used are: n-type doping level $4 \times 10^{14} \text{ cm}^{-3}$, $\phi_b = 0.79 \text{ eV}$ (B- NiSi_2). The precipitate concentration and radius are specific to each point and are shown in Fig. 5. As a result of the fitting, the measured diffusion length lies between the two calculated values or within experimental error from them, which can be considered a confirmation of the validity of the model.

In conclusion, a model of the carrier recombination process due to a precipitate with metallic properties in Si has been developed. It shows a good apparent agreement with experimental data. It was found that such precipitates can serve as very efficient recombination centers with minority carrier CCS in great excess of their geometric cross-section area and under certain conditions as large as, or slightly larger than the total CCS of their constituent metal atoms dissolved in Si. Under the weak generation conditions, the supply of minority carriers, via diffusion and drift, is the limiting factor of the recombination process.

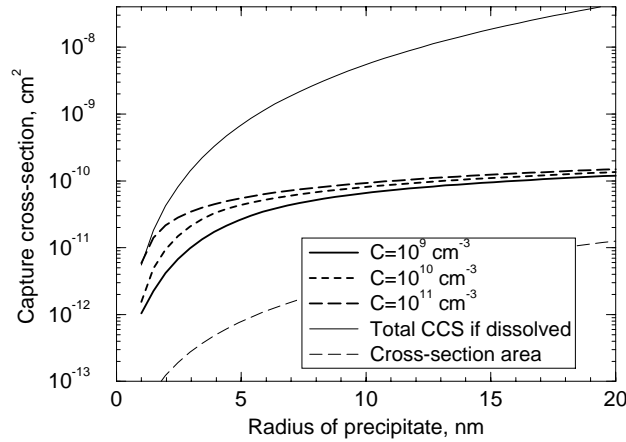


Fig. 4. Dependence of precipitate capture cross-section on its diameter at various precipitate concentrations. Other materials parameters used are the same as in Fig. 2.

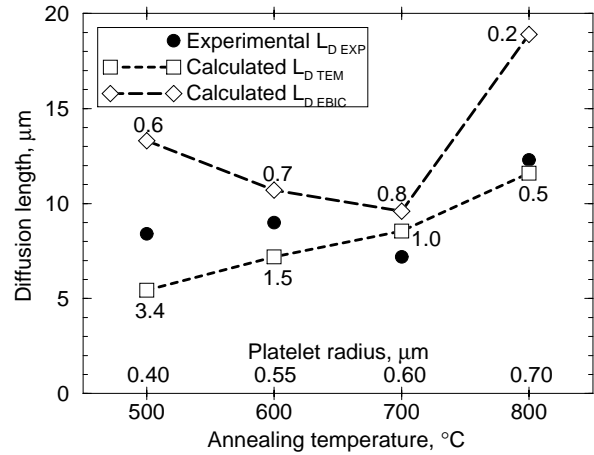


Fig. 5. Experimental and calculated hole diffusion lengths in n-type Si with NiSi₂ platelet-shaped precipitates. For each experimental sample, two values were calculated in accordance with two precipitate concentration values observed by TEM and by EBIC. The concentrations are indicated at each calculated point, in 10⁹ cm⁻³.

ACKNOWLEDGEMENTS

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Review of Light Degradation Research on Crystalline Si Solar Materials and Solar Cells

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The first paper on the light degradation of crystalline Si solar cells was published in 1973 when efficiency of solar cells using $1\ \Omega\cdot\text{cm}$, B-doped CZ silicon degraded under illumination and recovered by annealing around $200\ ^\circ\text{C}$. Recent research in the past ten years has showed that the light degradation caused by a formation of boron and interstitial oxygen complex with the deep energy level of $E_v + 0.35\text{eV}$ and $E_c - 0.45\text{eV}$. Two kinds of practical solutions to suppress the light degradation were successfully introduced: the usage of gallium impurity instead of boron and the reduction of interstitial oxygen by MCZ or annealing of the boron-doped CZ silicon at high temperatures. It was also pointed out that an optimization of the high temperature process is absolutely necessary for the boron-doped, oxygen-contaminated CZ silicon.

INTRODUCTION

Light-induced degradation of minority-carriers in B-doped silicon was firstly observed by Fischer and Pschunder in 1973¹. They reported that efficiency of cells fabricated using $1\ \Omega\cdot\text{cm}$, B-doped wafers degrades under AM0 simulated sunlight and the cell efficiency can be recovered by annealing at low temperatures above 200°C . Since then, the lower resistivity CZ wafers have been avoided in cell production although the low resistivity region can provide a higher efficiency. Corbett et al.² reported that lifetime degradation in CZ silicon is not due to a direct creation of defects by photons, but a dissociation of donor-acceptor defect caused by excess carriers generated by light irradiation. The lifetime degradation occurs not only under illumination, but also in the dark when forward bias voltage is applied to solar cells³. Schmidt et al. have attributed the light-induced lifetime degradation to an interstitial boron-oxygen pair created under illumination,⁴ since they have observed no degradation on n-type and gallium doped Cz silicon. The model was based on a similar annealing behavior of defect pairs of interstitial boron (B_i) and oxygen (O_i) intentionally created by electron irradiation⁵. However, the reported levels of the interstitial B_i - O_i defects could not be found by deep-level transient spectroscopy on non-electron irradiated Cz silicon. Nevertheless, the general correlation of the light-induced degradation with boron and oxygen could be proved by Glunz et al.⁶ by lifetime measurements on intentionally oxygen-contaminated FZ-silicon and experiments on a wide range of different Cz-materials. In particular, a superlinear increase of the defect concentration with the interstitial oxygen concentration was observed approximately to the power of five. Based on quasi-static lifetime measurements evaluated using the Shockley-Read-Hall theory, Schmidt and Cuevas⁷ reported that a deep recombination center created during illumination has an energy level between $E_v + 0.35$ and $E_c - 0.45\ \text{eV}$.

In 1997, domestic joint research was organized in Japan by Saitoh and Abe to understand the light degradation in more detail and to find a solution to suppress the light degradation. In 1999, the joint research was reorganized to an international level⁸. Various kinds of Si wafers were provided by Shin-Etsu Handotai Co. to the joint institutions including Sharp Corp., Hitachi, Ltd., Fraunhofer Institute for Solar Energy Systems, University of New South Wales, Georgia Institute of Technology and Tokyo University of Agriculture and Technology. On September 1999, the first workshop on light degradation was held in Sapporo to understand the degradation mechanism and to propose practical solutions to reduce the degradation. The joint research elaborated ways to suppress the light degradation of CZ materials and cells by using MCZ wafers with lower oxygen content and Ga-doped CZ wafers substituting boron as dopant^{8,9,10,11,12,13,14}.

After the first workshop, the research was directed to investigate the effects of high-temperature annealing conditions to reduce the degradation of the boron-doped, oxygen-contaminated CZ silicon¹⁵. At the second workshop on May 2000 in Glasgow, it was pointed out that an optimization of the high temperature process is absolutely necessary for the boron-doped, oxygen-contaminated CZ silicon¹⁶.

This paper provides the review on the light-induced lifetime degradation research on CZ silicon materials and solar cells. The practical solution without light degradation using Ga-doped CZ and B-doped MCZ Silicon is proposed as well as the importance of optimized annealing for the oxygen-contaminated,

boron-doped silicon. The Ga-doped silicon wafers are more suitable to fabricate extremely high-efficiency silicon solar cells.

LIGHT DEGRADATION OF CRYSTALLINE SILICON WAFER

After two decades from the first discovery of the light degradation by Fischer and Pschunder in 1973¹, German researchers reconfirmed the phenomenon through the research to fabricate highly efficient CZ Si solar cells^{3,6}. Under the assumption that the light-induced defect is totally activated under simulated sunlight for 30 hr and deactivated after a 200°C anneal, it is possible to determine the metastable defect concentration by the following equation⁶.

$$1/\tau_d - 1/\tau_0 = (v_{th}\sigma N_i + v_{th}\sigma_{res}N_{res}) - v_{th}\sigma_{res}N_{res} \quad (1)$$

where τ_d is the final lifetime after degradation, τ_0 the initial lifetime after the 200°C anneal, v_{th} the thermal velocity, σ and σ_{res} the capture cross section and N_i and N_{res} the concentrations of the metastable and residual defects, respectively.

During illumination, the wafers with resistivities ranging from 0.4 to 12 $\Omega \cdot \text{cm}$ degraded following an exponential time law described by the equation 2.

$$\sigma v_{th} N_i(t) = (1/\tau_d - 1/\tau_0) \{1 - \exp(-t/\tau_{gen})\} \quad (2)$$

The total defect concentration is a clear function of the boron concentration. The defect generation rate $1/\tau_{gen}$ increased monotonically with increasing boron concentration. The effect of boron concentration on the light degradation was clearly shown in Fig. 1 for the Cz-Si wafers with an interstitial oxygen concentration between 5.6 to $7.0 \times 10^{17} \text{ cm}^{-3}$. As indicated by the solid line in Fig. 1, there exists a linear relation between the defect and boron concentrations.

Using boron-doped Si wafers with a similar resistivity, the effect of interstitial oxygen concentration was investigated. The wafer surfaces were passivated with a corona-charged silicon nitride. Although some scatter is seen in Fig.2, the defect concentration is a superlinear function of interstitial oxygen concentration. The fitted solid line follows a potential power law of order five.

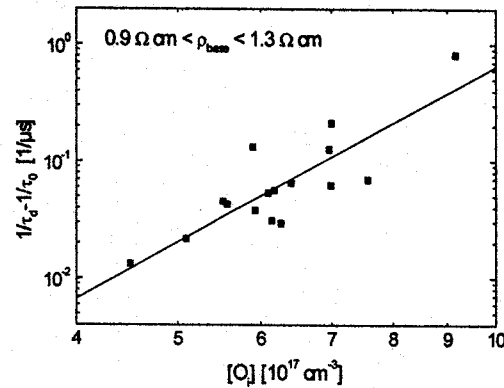
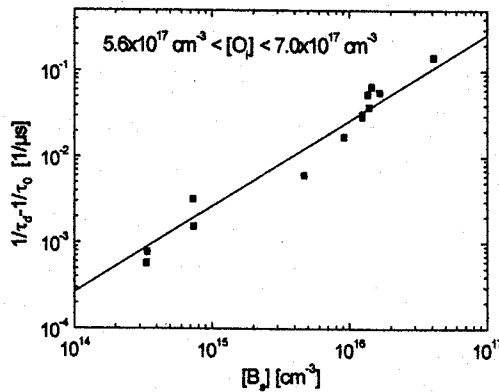


Fig.1 Defect generation rate vs. boron concentration in p-type CZ silicon⁶.

Fig.2 Defect generation rate vs interstitial oxygen concentration in oxygen-contaminated CZ-silicon⁶.

Based on lifetime data measured as a function of injection level, Schmidt and Cuevas studied electronic properties of the metastable defect⁷. In Fig.3, the measured dependences of $(1/\tau_d - 1/\tau_0)^{-1}$ on excess carrier concentration are shown by means of the contactless quasi-steady state photoconductance method¹⁷. The solid line curves fitted using the Shockley-Read-Hall theory showed that the fundamental recombination center created during illumination has an energy level between $E_v + 0.35$ and $E_c - 0.45$ eV and an electron/hole capture time constant ratio between 0.1 and 0.2. The deep-level center was ascribed to a new type of boron-oxygen complex.

Quite recently, a possible atomic structure for the defect proposed by Bourgoin et al. was a new complex consisting of one substitutional boron atom and three interstitial oxygen atoms¹⁸. The defect before

illumination is presumably a tight binding configuration illustrated by the state S in Fig.4. Under illumination or minority-carrier injection, electron is trapped at the defect inducing the Jahn-Teller distortion depicted by the metastable state M in Fig.4. The Jahn-Teller distortion generates the movement of the occupied levels to a deep energy. The model is consistent with the fact that a smaller or no degradation was observed in Ga-doped silicon. A Ga atom cannot accommodate three neighboring oxygen due to the larger atomic size.

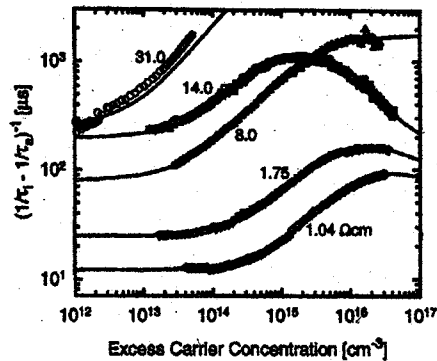


Fig.3 Injection level dependence of defect generation rate vs. excess carrier concentration for B-doped Si⁷.

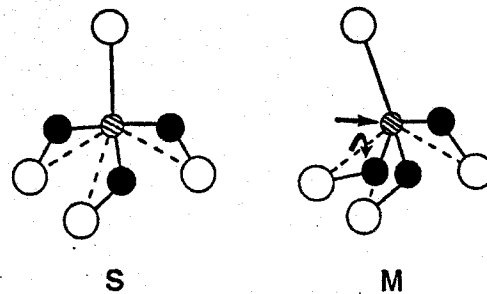


Fig. 4 Stable (S) and metastable (M) atomic Structures of one B₃-three O_i complex¹⁸.

ELIMINATION OF LIGHT-INDUCED LIFETIME DEGRADATION

(1) Reduction of Boron and Oxygen

The proposed model of the boron-oxygen complex suggests that light-induced lifetime degradation might annihilate by reducing the concentrations of either boron or oxygen. The expectation was confirmed through the international joint research⁸, in which various kinds of CZ, MCZ and FZ Si wafers were investigated (see Table 1). As shown in Fig. 5, the effective lifetime of conventional B-doped CZ wafers degraded to one tenth of the initial value after AM 1.5 simulated sunlight for 24 hr. The oxygen concentration in CZ silicon can be reduced to a 3 ppma level by controlling growth conditions in magnetic controlled CZ (MCZ) pulling. The reduction of the oxygen concentration suppressed the light-induced lifetime degradation as shown for the MCZ Si wafers of #3 to #5. The FZ Si wafer with an oxygen concentration less than 0.1 ppma showed no degradation^{9,11}.

Another idea was proposed by replacing boron with gallium atom as already indicated by preliminary results⁴. The Ga-doped wafers of #8 and #9 with a resistivity of 3 to 4 Ω cm showed a possibility to reduce light degradation^{10,11}. Ga-doped CZ wafers with a lower resistivity of 0.4 and 1.3 Ω · cm showed almost no degradation, although the oxygen concentration is as high as around 10 ppma. The result supports the boron-oxygen complex model for the light-induced lifetime degradation. It is noticeable that the obtained lifetime value is relatively high irrespective of the low resistivity.

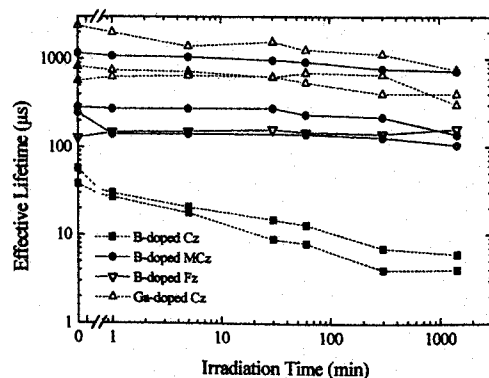


Fig.5 Variation of effective lifetime with AM1.5 illumination time for CZ, MCZ FZ silicon⁸.

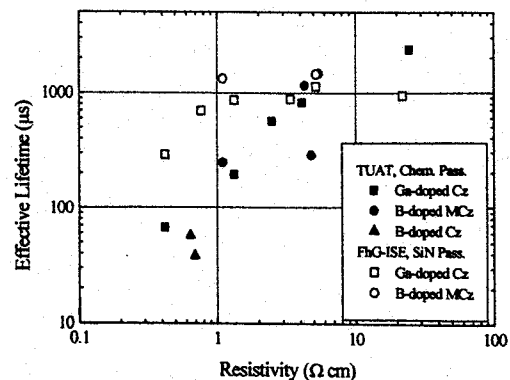


Fig.6 Carrier lifetime vs. resistivity for Ga and B-doped CZ silicon⁸.

As pointed out above, the effective lifetime for higherquality Si wafers depends strongly on the surfacerecombination velocity. Using the silicon nitride passivation technology, the Ga-doped wafers were found to show inherently high bulk lifetime^{8,24}. As shown in Fig.6, the bulk lifetimes were excellent even if the doping concentration was significantly high close to the theoretical limit by Auger recombination⁸.

By using the high-quality Ga-doped silicon, highly efficient silicon solar cells were fabricated to show about 22% even if the resistivity were as low as 0.2 to 0.4 $\Omega \cdot \text{cm}$. As shown in Fig.7, the efficiency values were even better or comparable to the ones on boron-doped FZ silicon and did not depend on the base resistivity. In addition, no degradation was observed for the gallium-doped CZ and also boron-doped FZ silicon cells. On the other hand, conventional boron-doped CZ cells degraded under AM 1.5 illumination.

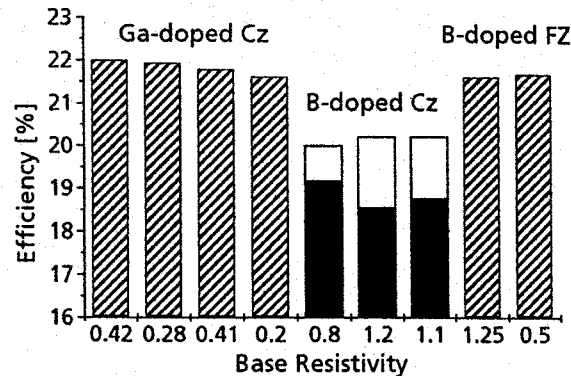


Fig.7 Efficiencies of the RP-PERC cells using Ga-doped CZ, B-doped CZ and B-doped FZ silicon. The closed columns show the results for B-doped CZ after Light degradation¹⁵.

(2) Optimization of Annealing Conditions

Degradation of cell efficiency due to lifetime degradation is not so high as it would be expected from the lifetime improvement during cell processing. Glunz et al. reported that an oxidation at 1050°C is effective to reduce the concentration of the metastable defect drastically. On average the stable lifetime after degradation is increased by a factor of 2 to 3 by the high-temperature processes⁶.

Based on the annealing effect, further study was carried out for boron-doped, oxygen-contaminated CZ silicon^{15,16}. A new anneal step was elaborated at medium temperature of 750 C for a short time of 10 min. As indicated in Fig.8, the defect concentration annealed at 750 C has the same effectiveness as the high temperature anneal of 1050 C/60 min step. The effect was almost the same for various boron-doped Cz-silicon with resistivities of 0.8 to 2.1 $\Omega \cdot \text{cm}$.

It was important to use optimized annealing process for these steps. Otherwise the lifetime and cell efficiency was severely reduced. As process parameters, ramp-up, plateau and ramp-down conditions at 1050 C oxidation were examined to study the effect on the lifetime. Fig.9 indicates the effective lifetimes after AM 1.5 for 48 hr illumination for the boron-doped and gallium-doped CZ, boron-doped MCZ and FZ silicon materials. After the unsuitable process A, lifetimes deceased significantly in all the oxygen-contaminated boron-doped and also gallium-doped CZ silicon. However, the optimized process B was very effective to have one order of magnitude higher than for process A. In contrast, MCZ and FZ silicon showed no sensitivity to the process schemes due to the low or no oxygen concentration.

The influence of the process A and B on cell performance were examined by applying the two schemes to two high-temperature oxidation steps in RP-PERC cell fabrication process. The resultant cell efficiencies for the various CZ, MCZ and FZ silicon are depicted in Fig.10 with the efficiency ratio in the lower graph. For the both boron and gallium-doped CZ cells, the stable cell efficiencies after AM1.5 for 48 hr by the optimized process B were much higher than the ones for the unsuitable process B. Oxygen-free FZ and MCZ with lower oxygen concentration showed almost no difference in cell efficiencies for the both processes.

In order to investigate the mechanism, the changes of the interstitial oxygen concentration were measured for the two processes from the absorption peak at 1107 cm^{-1} . As indicated in Fig.11, the oxygen concentration for the optimized process B was moderate and that for the unsuitable process A was lower

than that for the starting material. The strong reduction of the interstitial oxygen for the process A was speculated by the formation of SiO_2 precipitates.

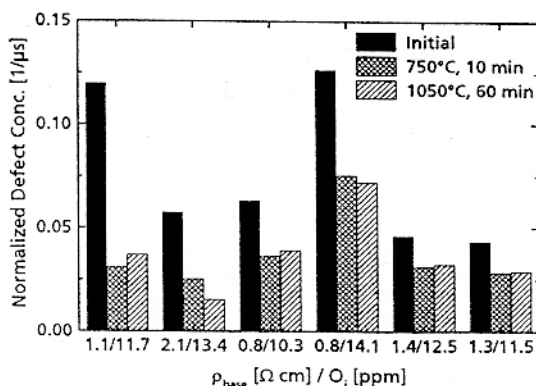


Fig.8 Defect concentration of B-doped silicon before and after two different anneal steps. Resistivity and oxygen concentration are indicated on the x-axis¹⁵

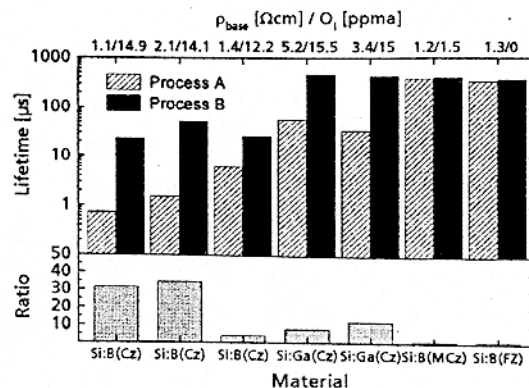


Fig.9 Lifetimes of B and Ga-doped silicon after 1050C oxidation with two different steps¹⁵

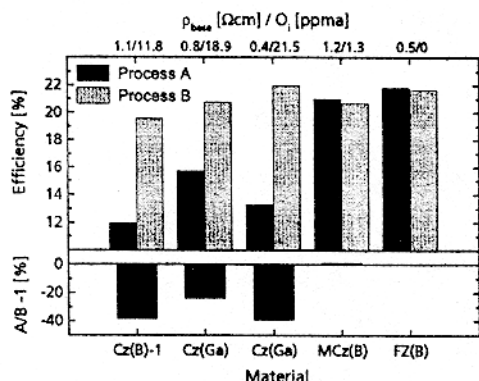


Fig.10 Effect of anneal steps of 1050C on cell Efficiency for B and Ga-doped CZ, MCZ and FZ¹⁶

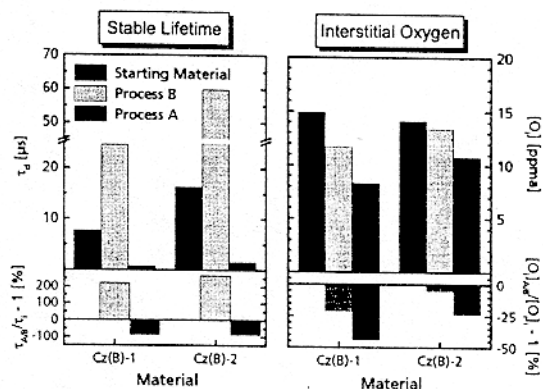


Fig.11 Correlation of process-induced lifetime changes (a) with changes of interstitial oxygen concentration (b)¹⁶

Table 1 Specifications of CZ, MCZ and FZ Si wafers employed for the international joint research⁸

Sample No.	Growth method and dopant	Resistivity ($\Omega \cdot \text{cm}$)	Oxygen content (ppma)
1	CZ, B-doped	0.64	8.21
2	CZ, B-doped	0.69	14.5
3	MCZ, B-doped	4.80	11.9
4	MCZ, B-doped	1.07	3.28
5	MCZ, B-doped	4.33	2.93
6	FZ, B-doped	0.60	<0.1
7	FZ, B-doped	3.98	<0.1
8	CZ, Ga-doped	2.49	9.45
9	CZ, Ga-doped	4.12	10.5
10	CZ, Ga-doped	9.61	9.61
11	CZ, Ga-doped	0.42	10.0
12	CZ, Ga-doped	1.33	10.0

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Characterizing the Impact of Point Defects/Dopants/Impurities on Defect Nucleation/Growth/Gettering and Si PV Performance

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The objective of this presentation is to stimulate an open and interactive discussion based on the status in 2000 on those topics; namely, point defects, impurities, gettering, etc., which actually served as the basis for this annual workshop when it was first held in 1990. Thus, we will initiate and illustrate a diverse sequence of crystalline silicon issues from vacancies to grain boundaries with the hope of arriving at a somewhat overly ambitious, but highly desirable Year 2000 materials science/ PV device triage which will:

- i) reinforce what basic “defect” related silicon materials science is currently firmly understood, particularly with regard to how high performance PV devices may be beneficially impacted,
- ii) identify unresolved and emerging materials processing/characterization/supporting simulation issues which merit a focused allocation of currently available resources, and
- iii) examine mechanisms for identifying/incorporating higher risk/longer term materials research topics into the goals of NREL’s *Beyond the Horizon* or similar initiatives.

In order to get the discussion started we will present several highlights of phenomena primarily related to vacancies(interstitials), oxygen(nitrogen), their mutual interactions, and their role when Ga or Sn are added to CZ Si. We start our overview by reviewing the impact of internal vacancy/void formation, localized oxygen precipitation, and interstitial oxidation-induced stacking(OSF) fault formation in wafers containing an OSF-ring. Since large diameter Czochralski silicon crystals contain a nonuniform defect distribution across an individual wafer diameter, as well as along the crystal growth axis, they provide a model system for examining the behavior of point defect/impurity interactions and they initially influence minority carrier lifetime and ultimately PV device efficiency. More specifically, as-grown CZ wafers often contain a central “D-defect” (vacancy-dominant) zone which is separated from an outer (interstitial-rich) region by an annular ring containing SiO₂ precipitates. After oxidation the annular OSF- ring, contains a high density of oxidation stacking faults. The position of the OSF-ring under various crystal growth and wafer heat treatments has been extensively described both experimentally[1] and theoretically[2]. The mechanism for formation of the OSF-ring is generally agreed to be controlled by the interaction of vacancies/interstitials and oxygen during post-solidification cooling. For example, one model for OSF-ring formation is based on the presence of a higher vacancy concentration on solidification, followed by a sequence which includes a strong radial interstitial out-diffusion and annihilation via Frenkel pair recombination. This favors the formation, particularly in the center of large diameter ingots, of nuclei consisting of vacancy/oxygen complexes. The V-O nuclei can operate in either of two modes[3] depending on their size; one of which enhances the condensation of vacancies into octahedral voids, while the other initiates the formation of nanoscale SiO₂ precipitates. A

subsequent annealing enables growth of the internal oxide precipitates, whose expansion locally ejects Si interstitials to form the OSF-ring.

The importance in understanding the above sequence lies in its value in spawning defect engineering options for crystalline silicon devices. For example, modeling of more subtle components of OSF-ring wafers, which include radial zones with anomalous oxygen precipitation (AOP) and a band of defect free silicon, has led to the commercial offering of a “Magic” Denuded Zone (MDZ) wafer for the IC market[1], and the introduction of nitrogen as a modulator of the silicon point defect dynamics in yet another new wafer product[4]. Even though MDZ wafers are likely to negatively influence PV devices, where bulk SiO₂ precipitates functioning as gettering sites will degrade the minority carrier lifetime, the basic phenomena does open up new possibilities for studying the complexing of vacancies with dopants/oxygen/metallic impurities. Following this theme we consider first the impurity nitrogen, which exists as a N₂ pair in Si, and is believed to be electrically inactive[5], quite different from the other group V elements. A great deal of new information has appeared in the past two years—mostly by Japanese wafer suppliers[6]—reporting that nitrogen can suppress void formation, enhance the nucleation rate of SiO₂ precipitates, and increase wafer mechanical strength by blocking dislocation motion. Naturally, much interest lies in studying the N-V pair[6], as well as the electrically active signal available for nitrogen by its interaction with oxygen to form shallow thermal donors[7], which influence subsequent oxygen precipitate internal gettering. How this V-O-N activity will impact high end PV substrates remains to be seen, but scientifically it should also be viewed in conjunction with point defect issues associated with recent work on Sn[9,10] and Ga[11] doping of silicon, as well as with Al gettering[12]

Along these lines, we consider next silicon crystals doped by group IV isovalent impurities which have attracted strong interest; particularly for Si-Ge alloys suitable for device bandgap engineering. In addition, small concentrations of isovalent C and Sn on substitutional lattice sites play a subtle and potentially useful role, since their large lattice misfit with silicon causes them to generate and interact with native point defects, which subsequently complex with and getter impurities. Because of its small size, most work on carbon has been in the context of interstitials, which are critically important in reducing the transient enhanced diffusion (TED) component of boron-doped shallow junction IC devices[13]. Although there are fewer examples for tin-doped silicon, it has been reported that the concentration of V-O pairs, known as A-centers, is reduced by a factor five in highly Sn-doped Si following electron irradiation[14]. Also, since Sn essentially suppresses the generation of oxygen-containing thermal donors, it is likely to influence the oxygen precipitation process[15], following the concept[16] that homogeneous oxygen precipitate nucleation is coupled to thermal donor formation. This raises the possibility of using Sn-doped material for controlling oxygen precipitation, as well as thermal donors, via the generation of Sn-V pairs.

Moving on to gallium doping as a means for controlling the light degradation of low resistivity CZ wafers, we finally come closer to actual PV performance issues. This topic illustrates the uniqueness and strong influence specific oxygen pairs have on carrier lifetime and cell efficiency. Although this topic was reviewed last year at this workshop by Saitoh[10] in the context of the International Joint Research Effort, and additional work has since been published by the FhG-ISE/SEH group[9], there are still questions about whether point defect engineering using vacancies, and/or Sn, can be beneficially folded into the activity, particularly with regard to the gap between the maximum achievable CZ and FZ/MCZ cell efficiencies.

At NCSU we have recently been configuring MeV ion implantation experiments on CZ and epi-Si as a means to:

- i) spatially separate vacancies and interstitials, i.e. voids and dislocations, so that what occurs radially for ingot growth can be “reproduced” on a wafer surface,
- ii) examine the impact of background oxygen/nitrogen concentrations on oxygen precipitation and point defect/impurity interactions,
- iii) use these structures to explore the mechanisms and stability of gettering for different metals.

Also, stimulated by the recent NREL *Beyond the Horizon* PV initiative, and as a wrap-up for the discussion on point defect engineering, we present an approach to using vacancies/dislocations/grain boundaries as elements in high performance Si solar cells. This novel nano-cavity device, one element of which is shown in Fig. 1(a), is based on using open volume void defects which have been decorated with metallic impurities and interconnected with

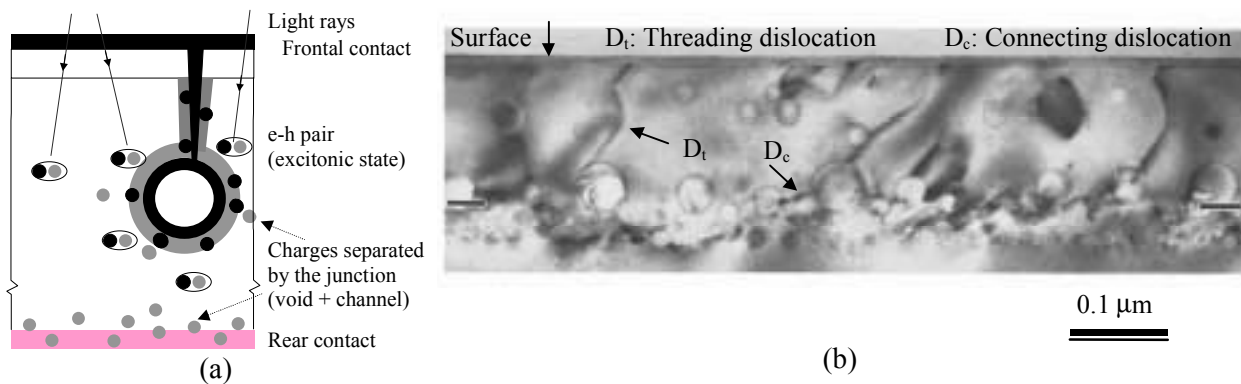


Fig. 1: (a) Schematic representation of a nanovoid and threading dislocation processed to form a diode, and (b) Cross-section TEM image[18]¹ of helium implanted $\text{Si}_{0.86}\text{Ge}_{0.14}/\text{Si}$ heterostructure with lateral and threading dislocations connecting voids with each other and the top surface.

dislocations, see Fig. 2(b). The local point and extended defect concentrations surrounding these structures can be controlled surprisingly well using ion implantation techniques[17]. It may be viewed as a negative array of the diode ball PV concept initiated at Texas Instruments some years ago[19], only in our configuration the balls are voids held together by the silicon lattice.

In support of engineering these defect layers we have at our disposal a number of tools which can provide us with “snapshots” of the entire spectrum of extended defects expected in crystalline Si; thereby enabling us to manipulate the defect and study their interactions. One knowledge-based fallout goal of this effort is to generate a sample set which will enable the quantification, calibration and comparison of empty volume defects/electrically active defect complexes/nanoscale imaging via Positron Annihilation Spectroscopy (PAS)[20], Deep Level Transient Spectroscopy (DLTS), and Transmission Electron Microscopy (TEM) data. A range of defect sizes from point defects to extended defects can be systematically introduced[21] via ion implantation into Si with high (Cz – with and without an OSF-ring), and low (Epi) levels of interstitial oxygen.

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Impurity and Defect Characterization in c-Si by Positron Beams

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Abstract:

Positrons are a unique probe of defects and their chemical and electronic environment. Being the antiparticle of the electron they can get trapped at defects, which are either negatively charged or neutral or present some form of open volume such as vacancies. The electron momentum distribution at and near the defect is distorted compared to the defect free crystal. When a positron experiences its ultimate fate, annihilation with an electron, the emerging gamma ray photons carry, encoded, this change in momentum distribution and can be analyzed to reconstruct the type of defect at the annihilation site. No sample preparation is necessary. The use of monoenergetic beams of positrons allows depth profiling of such defects from the surface down to several micrometer depth, a region crucial for most applications involving silicon. The various versions of positron annihilation spectroscopy are described and illustrated with examples from recent works.

Introduction

Silicon is the foundation of almost all electronic and electric applications ranging from analog transistors to the building blocks of computers and on to electric power generating photovoltaic cells. Across the board defects stand between the performance of real devices and what is theoretically possible. With a continuing trend to smaller dimensions defects will play an even more critical role. In order to either take advantage of defects or to eliminate them, a detailed understanding about their evolution and characteristics is vital. For this probes are needed to characterize these electrically active defects with high sensitivity down to parts per billion. Many such tools have been developed and optimized for this task.

In an ideal world such a diagnostic tool has to be sensitive to the defects that influence the device performance only. It should be sensitive down to a lower limit when the defect in

question no longer hampers device performance (currently parts per billion). The information extracted should completely characterize the defect and its immediate environment. Ideally the sample material volume, which does not contain any defects, should be “invisible” to the technique and little or no “sample preparation” (typically destructive) should be involved. The active volume of solar cells is typically no thicker than a micrometer. Any technique should be surface and near surface sensitive down to that depth. The capability for depth profiling and spatially resolved data is desirable.

The various versions of positron annihilation spectroscopy (PAS) can provide additional unique information to add more pieces to the puzzle. PAS fits some of the criteria for an ideal probe. In silicon (as in other semiconductors) positrons behave very much like holes. This includes their response to defects. Positrons “like” certain type of defects. They get trapped at neutral or positively charged sites. Once implanted in a sample at an energy dependent on the initial incident energy, the positron will sample a volume characterized by its diffusion length, and, if trapping defects are present, get trapped there. The local electron density and momentum distribution have a small but measurable effect on the eventual annihilation of the positron. Upon annihilation, predominantly two photons emerge in near opposite direction, which carry away the combined momentum of the electron positron pair and their rest mass energy. The electron momentum will cause small angular deviations from antiparallel emission and Doppler shifts in the energies $E_{1,2}$ of the photons. The positron, being the only particle of its kind typically resides in its ground state. Its contribution to the Doppler shifts and angular deviations can be neglected. The density of electrons determines the lifetime of the positron. All three parameters, angular deviations on the order of milliradians, typical Doppler shifts away from the rest mass energy of 511 keV on the order of 1 keV, and changes in the lifetime away from 220 picoseconds can easily be resolved with modern detection technology.

At defects the distribution of high momentum electrons (such as those bound to the ion cores) and low momentum electrons (as the conduction band electrons) changes. At a vacancy site, less bound core electrons (from the missing ion core) are available. On average, annihilations from this site carry less Doppler shift. The momentum distribution of the electrons bound to neighboring atoms retains a component typical for the elemental type of the atom and the chemical bond between atoms. With increasing binding energy the elemental-specific character increases. Photons with large Doppler shifts carry this information. Also, the electron density drops and the positron lifetime, as a result increases. In figure 1 the effects of element specific changes are indicated.

We will discuss the capabilities of this tool in general and provide a number of recent works selected to illustrate both the scope and sensitivity of the technique. The incident energy of the positron when it impinges onto a sample, determines its mean implantation depth. Thus, with a variable energy monoenergetic positron beam, the implantation depth can be scanned. A typical laboratory positron beam with an energy range from 0 to 100 keV can sweep across the depths of interest.[Coleman book][Krause-Rehberg book][P.J. Schultz, K.G. Lynn, Rev. Mod. Phys. **60** 701 (1988)]. The energy required for a mean depth of 5 μm is just under 35 keV for silicon. The positron beam can be focused to smaller cross sections of several micrometer diameter, given enough initial intensity.[A.P. Mills, jr, Appl. Phys. **23**, 189 (1980)][W.E. Frieze, D.W. Gidley, K.G. Lynn, Phys. Rev. B **31**, 5628 (1985)][K.F. Canter in “*Positron Studies of Solids, Surfaces, and Atoms*” A.P. Mills, jr, W.S. Crane, K.F. Canter, eds, (World Scientific, Singapore, 1986) p. 102] Angle resolved measurements suffer from small detector solid angles and require bright and

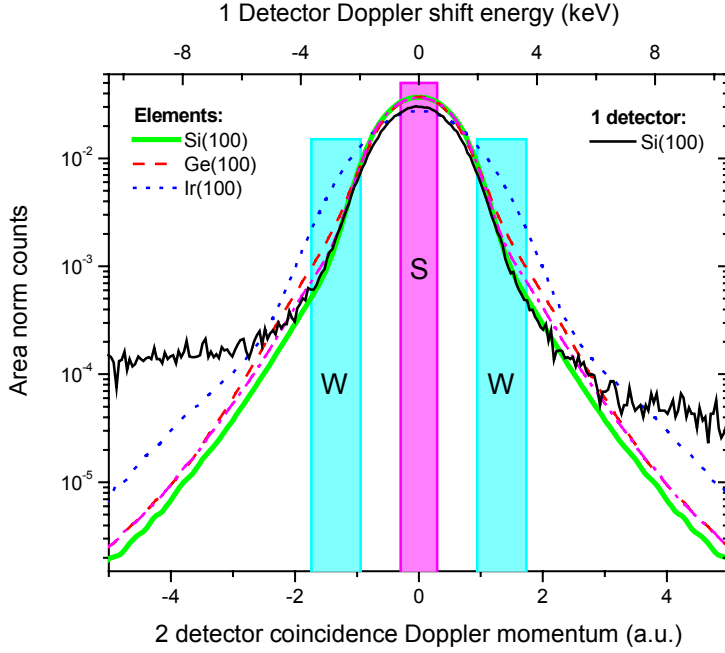


Figure 0 Doppler broadening of the 511 keV electron-positron annihilation line for Si as observed with one detector (upper x-axis in keV photon energy) and 2 detectors in coincidence (lower x-axis in atomic momentum units). The axes are adjusted to match the results for Si. In the two-detector case data for Ge and Ir crystals are shown to illustrate the sensitivity to element-specific effects (see text). The shaded regions are the energy windows used to evaluate the standard 1 detector S and W parameters. The resolution of the two-detector system is 0.605 a.u. as measured with the 514 keV line from ^{85}Sr , which is about the width of the S-window.

intense positron beams available only in a few laboratories. Doppler broadening measurements, where many detected Doppler shifted photons broaden the photon line at $m_0c^2 = 511$ keV (m_0 is the rest mass of the electron/positrons), can be carried out in less than an hour for on depth scan. Detailed discussions of positron annihilation spectroscopies can be found in Refs. [P.J. Schultz, K.G. Lynn, Rev. Mod. Phys. **60** 701 (1988)][in “*Positron Spectroscopy of Solids*” A. Dupasquier, A.P. Mills, jr., eds, (IOS Press, Amsterdam, 1995)]

The incident positron will rapidly loose its kinetic energy during the initial implantation to electronic excitations and finally phonon scattering. This thermalization time takes on the order of one picosecond.[A. Perkins, J.P. Carbotte, Phys. Rev. B **1**, 101 (1970)] For the

remainder of its lifetime (typically 220 ps in defect free single crystal silicon) it will diffuse through the material and possibly trap at a defect site. Upon annihilation with an electron into two photons of energies $E_{1,2}$ the momentum of the electron is translated into a Doppler shift.

$$E_{1,2} = m_0c^2 - E_b + T \pm 1/2 p_{\parallel}c \quad (1)$$

Typically the binding energy of the electron E_b and the remaining kinetic energy of the positron T are negligible compared to the rest mass energy m_0c^2 ($E_b, T \ll m_0c^2$). Decays via three photons when the spins of electron and positron are aligned (and higher orders) are possible but occur at a rate of $<1/370$ compared to two photon decays as long as spin polarization does not play a role.[A. Øre, J.L. Powell, Phys. Rev. **75**, 1696 (1949)] Averaged over a large number of detected Doppler shifted photons the annihilation line at m_0c^2 broadens. Traditionally, the shape of the annihilation line is parameterized into S and W. The former, S, is defined as the number of detected photons in a narrow central region of the photo-peak, typically with the width comparable to the resolution of the used detector (1 to 1.5 keV), normalized with the total counts in the peak. The latter, W, is defined as two equally wide regions (also 1 to 1.5 keV typically) in the “wings” of the peak, one on either side, and also normalized with the total peak counts. While S is sensitive to annihilations with small Doppler shifts (i.e. annihilations with low momentum conduction electrons), W relates to large shifts (i.e. high momentum, bound

electrons). While there is some correlation between these parameters, changes in high momentum Doppler shifts caused by differences in the chemical bond or the element type of the binding ion core predominantly change W , while S “sees” only conduction electrons spilling over into open volume traps for positrons (see fig 1). As the size of the open volume increases from mono vacancies (not stable in Si at room temperature) to di-vacancies and larger, the value of S (W) increases (decreases) in steps. The changes in S and W relative to defect free bulk Si carry the information on open volume; absolute values of S and W are system and resolution dependent.

One topic of interest is the re-crystallization of single crystal silicon after it was amorphized by ion bombardment. It is known that the re-growth (solid phase epitaxy (SPE)) occurs from the back end interface where the damaged layer connects to the undamaged original crystal. The speed of growth is influenced by the presence of impurities and dopant atoms. These can combine with defects such as vacancies to complexes, which in turn hinder or further the re-crystallization process. Also impurities may “get stuck” at the growth front and move along to the surface of the material, thereby changing the implanted dopant profile. Doppler broadening positron annihilation was used to investigate this process.[C.M. Chen, S. Rassiga, Th. Gessmann, M.P. Petkov, M.H. Weber, K.G. Lynn, H.A. Atwater, MRS conference proceedings, MRS spring 2000 meeting San Francisco (2000), to be published] FZ grown samples were amorphized by $^{29}\text{Si}^+$ ion implantation at LN_2 temperature with or without additional dopant implantation of phosphorous and together with boron. The implantation energies were chosen to create the same depth profiles. Subsequently the samples were partially re-crystallized for different times at 600°C such that the growth front has advanced the same distances.

Figure 2 shows the result of positron annihilation measurements (one detector) for three samples at different stages of the SPE process. In the first annealing step when the growth interface advances to 208 nm depth the abundant amount of open volume in the amorphous Si network is reduced in general. During further annealing the interfaces advances to the surface of the sample, which can be seen as the dip Doppler signal ($S_{\text{normalized}}$) moves to lower depths. Some open volume defects remain at the original interface depths and a decrease below the defect free value ($S_{\text{normalized}} = 1$) at the surface remains. The latter is related to oxide at the surface. The slope in the Doppler signal at the interface depends on the dopant and is steepest for P doping, indicating the formation of P-V complexes.

At the expense of signal intensity, two detectors can be used in coincidence to detect both photons from individual positron annihilation events. This greatly reduces the background under the photo peak. The effects due to the chemical environment of a defect and the elemental type of nearest neighbors can be identified clearly. Systematic effects such as pile-up of independent events occurring on close proximity in time and incomplete charge collection in the detector are suppressed as well as random signals independent of positron-electron annihilations. If the second detector also has good energy resolution equal to that of the first, the signal to noise ratio improves further to a factor of about 1000 over a single-detector system. Further, and more importantly, the difference in energy of the detected photons is the full Doppler shift (compared to only half on average when one detector is used only), convoluted with the combined resolution of the detectors.

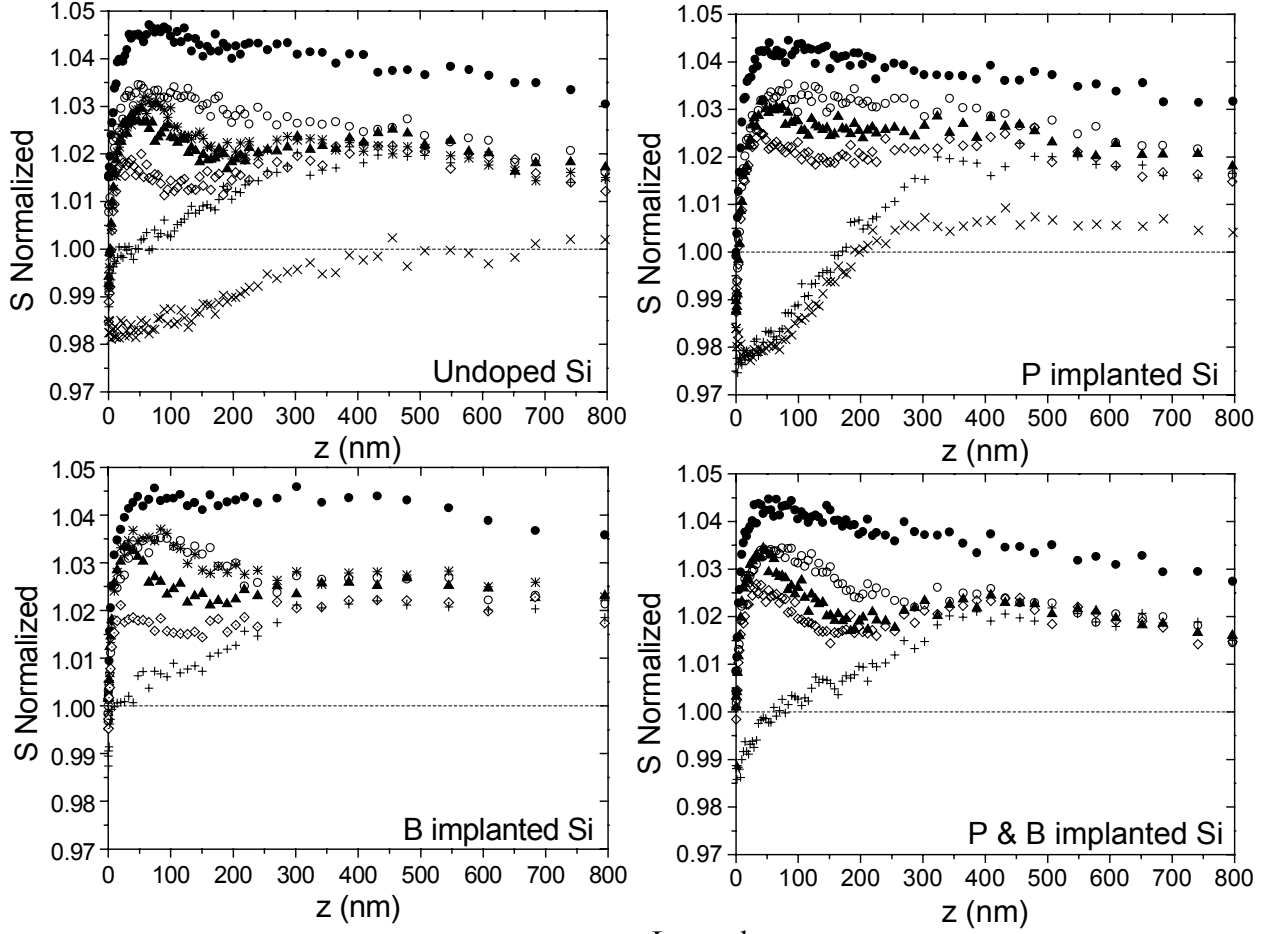


Figure 2. Positron annihilation spectroscopy (PAS) data for undoped, P-, B-doped, and P&B-doped silicon samples. The different curves for each sample include an as-implanted sample (interface at 346 nm), annealing steps with the interface at depths given, a fully crystallized sample, and a fully crystallized sample with an additional 800°C anneal, to anneal out defects in the end-of-range damage region from the ion implantation.

Legend:

- as implanted
- interface depth, 208 nm
- * interface depth, 139 nm
- ▲ interface depth, 69 nm
- ◇ interface depth, 35 nm
- + fully crystallized
- × fully crystallized with 800 C anneal

$$\Delta E = E_1 - E_2 = p_{\parallel} c \quad (2)$$

While the resolution of the detector system is $\sqrt{FWHM_1^2 + FWHM_2^2} \approx \sqrt{2} \cdot FWHM$ (if the detectors have equal resolution), the detection of the full Doppler shift effectively improves the resolution by a factor of $1/\sqrt{2}$. If pile-up or incomplete charge collection or other systematic effects occur when the photons are detected, this tends to shift the sum of the energy of the photons away from $2 m_o c^2$.

$$\Sigma E = E_1 + E_2 = 2m_o c^2 - E_b + T \approx 2m_o c^2 \quad (3)$$

Most notably, Doppler shifts cancel out of the sum energy, and when electron binding energies and positron kinetic energies are small (as is typical), the sum energy spectrum is a direct measure of the system resolution. When the data are collected in a two-dimensional histogram, the regions outside of a narrow window centered at $\Sigma E = 2 m_0 c^2$ can be used to evaluate the residual background.

From the coincidence data, a Doppler histogram can be extracted that shows counts for a particular Doppler shift as a function of Doppler shift (of course convoluted with the system resolution). Such a histogram spans more than six orders of magnitude in counts per bin. To see small variations due to changes in the nearest neighbor of defects or due to chemical bond variations it is suitable to compare a spectrum in question to a reference spectrum of a similar sample. Typically one computes the ratio of counts in each bin. When the density of states for a particular momentum increases, this will cause peak like structures in the ratio curves. The location of the peaks can be used to identify the element, which caused this change. Examples of this are shown in Figure 3. The ratio of Doppler data (two-detector coincidences) to data from Al(100) are computed. The choice of Al is somewhat arbitrary but since theoretical models work very well for Al, this choice of a reference element will include no additional complications.

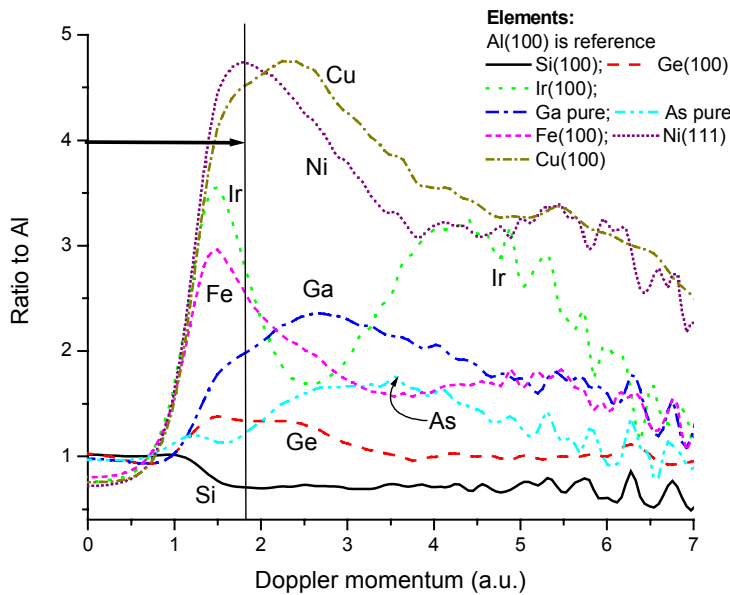


Figure 3 Ratio of two-detector coincidence data to data from Al. Because of the symmetry about 0 a.u., only the positive side is shown. The vertical bar at 1.74 a.u. indicates the outer edge used in one-detector measurements.

implanted amorphized Si, as well as from theoretical calculations. This work lays the foundation for PAS studies of impurity-defect related processes in *a*-Si:H. With the use of only one detector the lack of signal-to-noise ratio in the wings of the annihilation line allows the experimenter only to distinguish between the neutral and the negatively charged dangling bond state (D^0 and D^-). The results are shown in figure 4.

This technique was employed to identify the phosphorus-defect complex ($*D^-$) in *n*-type hydrogenated amorphous Si (*a*-Si:H). [M.P. Petkov, M.H. Weber, K.G. Lynn, R.S. Crandall, V.J. Ghosh, Phys. Rev. Lett. **82**, 3819 (1999)] One of the nearest neighbor atoms of a dangling bond in amorphous Si is replaced by a phosphorous donor atom. Positrons are attracted and localized at the small open volume associated with the dangling bond defects, particularly when it is in the negative charge state D^- . The radiation detected after annihilation gives a characteristic P-signature, regarded as a $*D^-$ ‘fingerprint’. Additional evidence is obtained from a comparison to P-

In the experiment intrinsic and n-type amorphous Si samples were prepared at the National Renewable Energy Laboratory (NREL) by glow discharge chemical vapor deposition (GD).

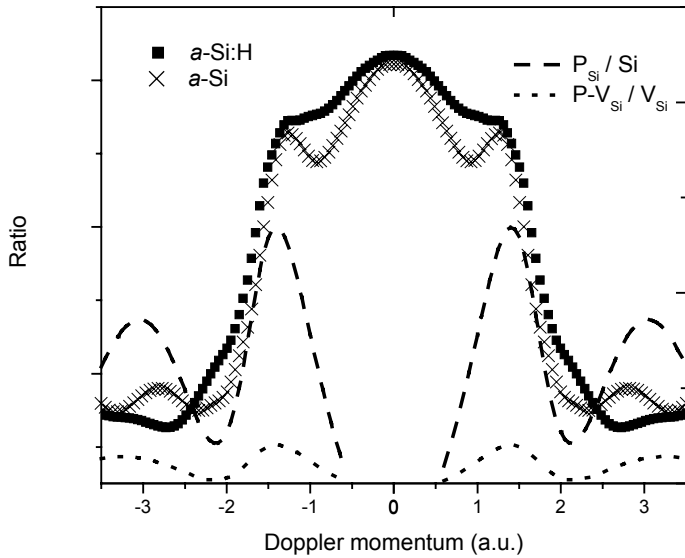


Figure 4 Ratio of a sample with high phosphorous content to one without P of amorphous Si and theoretical model calculations. (★) are glow discharge samples and (×) are amorphized by ion implantation. The dashed and dotted lines are theoretical model calculations of P replacing Si on a Si lattice vs. Si and a P-V_{Si} complex vs. a V_{Si} vacancy site in Si respectively.

where on P atom replaces a nearest neighbor of a Si vacancy to a simple Si vacancy and where P atoms replace all Si atoms in a Si crystal. In a third configuration the P atoms sits near a neutral dangling bond site. The location of the peak in the experimental data fits the location of the peak in the theoretical models, confirming that P sits near the positron annihilation sites, which in turn are the slightly negative open volume areas of the dangling bonds.

Another project involves the investigation of impurity gettering in CZ and FZ grown silicon. With increasing temperature impurities become increasingly mobile in silicon and can diffuse throughout the material to the surface or get trapped at defects. However, with increasing temperature their solubility also increases, effectively limiting the temperature to a maximum allowed for a given upper limit of an impurity concentration. This, in turn will limit the distance an impurity will travel. Of particular concern are transition metals like iron, which will not reach an external surface in practical times. Alternatively, layers of defects can be introduced by Si-ion bombardment followed by an annealing step. At the projected range of the ions R_p an interstitial rich layer is formed while at approximately half that range $R_p/2$, excess vacancies are created. It was found that depending on the concentration of oxygen present in the material or not (CZ vs. FZ grown Si) Fe is gettered at R_p only or at R_p and at $R_p/2$, respectively. While the nature of the defects at R_p has been resolved (with TEM for example), their type remains unclear at $R_p/2$. Some kind of defect complexing involving Fe and a vacancy or di-vacancy is hypothesized, which is then suppressed by the presence of oxygen in the material. Data are shown in figure 5.

Again positrons may shed light on this problem. One-detector Doppler broadening was applied to similar samples. However, any possible change due to gettering was offset by the

Typically, the latter contains about 9 at. % H. For comparison FZ grown n-type Si was amorphized by ion implantation with 200 keV $^{29}\text{Si}^+$ to a fluence of $1 \times 10^{16} \text{ cm}^{-2}$. The *a*-Si structure was subsequently relaxed at 500°C for 2 hours. A P-rich *a*-Si version of this sample was produced by $^{31}\text{P}^+$ implantation (200 keV, $1.7 \times 10^{15} \text{ cm}^{-2}$) of FZ-Si(100) following a $^{29}\text{Si}^+$ implantation (150 keV, $1 \times 10^{15} \text{ cm}^{-2}$). This sample was not subjected to a structural relaxation.

The ratios of Doppler histograms for the P rich and undoped samples were computed for the GD grown and ion implanted sample sets respectively. These were then compared to theoretical calculations. The calculations compared scenarios

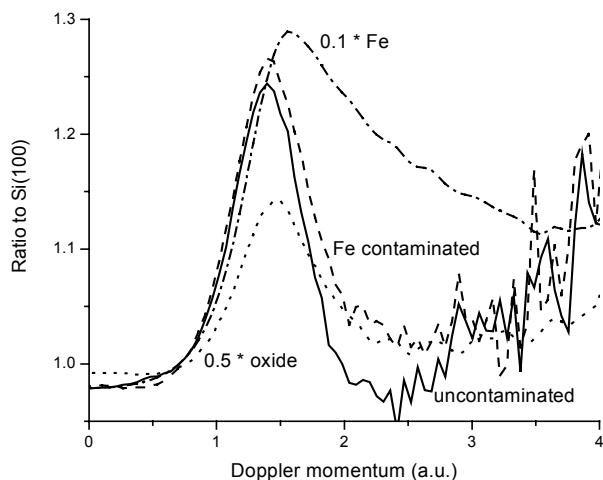


Figure 5 Fe contamination and gettering at ion implantation produced defects in CZ grown Si. In this preliminary work oxygen is clearly visible at 1.5 a.u. and iron appears to cause a small increase in the valley at 2.3 a.u. The solid line is from uncontaminated and the dashed line from Fe contaminated Si. The dotted line is the oxygen signal and the dot-dashed line a scaled version of pure Fe, all in ratio to Si.

effect of surface SiO_2 present during the implantation.[M.P. Petkov, C.M. Chen, H.A. Atwater, S. Rassiga, K.G. Lynn, *Appl. Phys. Lett*, (2000)] The implantation process transports oxygen into the sample and causes large changes in the positron signal.[R.A. Brown, O. Kononchuk, G.A. Rozgonyi, S.V. Koveshnikov, A.P. Knights, P.J. Simpson, F. González, *J. Appl. Phys.* **84**, 2459 (1998)] Here, samples of CZ and FZ grown Si have been Si ion implanted at 2 MeV. They were partially contaminated with Fe (100 keV implantation from the back side) and subsequently annealed at 900 °C to create the gettering layer and to mobilize the Fe impurities. The samples were studied by SIMS and by positron annihilation with two detectors in coincidence. The gettering layers resulting from 2 MeV implantation are estimated to be at $R_p =$

2.05 μm and at $R_p/2 = 1.0 \mu\text{m}$ respectively. The SIMS data clearly show the increase in Fe concentration at these depths. The positron data, however, cannot be interpreted conclusively to date. Several aspects contribute to the difficulties. First, the gettering layers are rather thin ($\approx 0.2 \mu\text{m}$), while the positron implantation profile is much broader at the energy required to reach 2 μm . Second, positrons are less sensitive to interstitial sites and may not “see” the defects at R_p . Third, the contribution to the positron histograms due to oxygen in the samples is large, even for the FZ grown sample and also when the samples were HF dipped prior to the implantation step, and may obscure the effect due to Fe. Further the peak in the ratio location curve expected from Fe is very close to the peak location for oxygen.

To address these issues a number of steps are taken. Samples with identical histories except for their contamination will be used. Temporarily, Fe will be replaced by copper atoms as the contaminating element. And finally the samples will be etched to remove the top layer in successive steps to enhance the depth resolution of the technique.

Positron lifetimes can be extracted by measuring the elapsed time between a suitable start signal and the detection of an annihilation photon.[F. Becvár, L. Lesták, I. Novotný, I. Procházka, F. Sebesta and J. Vrzal, *Mater. Sci. Forum* **175-178**, 947 (1995)] In most cases the start signal comes from the positron source, the radioisotope ^{22}Na which decays via a short lived intermediate excited state of ^{22}Ne . With a lifetime of several picoseconds the neon atom de-excites by emission of a 1.27 MeV photon. Its detection triggers the start. However, the positrons emitted from the source isotope have a very broad energy distribution up to 0.6 MeV, unsuitable for studies of thin films and near surface effects. The correlation of the 1.27 MeV “start” photon with the detection of the positron annihilation in the sample is equally impractical because of the inefficient conversion process of creating a monoenergetic beam. One alternative solution is to extract secondary electrons knocked out of the sample when the positron impinges on it or to

generate a pulsed beam. Either method has been implemented [D. Schödlbauer, P. Sperr, G. Kögel, W. Triftshäuser, “*Positron Annihilation*”, P. C. Jain, R. M. Singru, K. P. Gopinathan, eds. (World Scientific, Singapore 1985), p. 957][R. Suzuki, Y. Kobayashi, T. Mikado, H. Ohgaki, M. Chiwaki, T. Yamazaki, T. Tomimasu, Mater. Sci. Forum **105-110**, 1993 (1992)][J. S. Nico, D. W. Gidley, A. Rich, P. W. Zitzewitz, Phys. Rev. Lett. **65**, 1344 (1990)][K. G. Lynn, W. E. Frieze, P. J. Schultz, Phys. Rev. Lett. **52**, 1137 (1984)] and time resolutions of better than 350 ps were reported.[S. Szpala, M.P. Petkov, K.G. Lynn, to be published (2000)] This is sufficient to extract defect dependent changes in lifetimes of positrons in silicon.

Recently a beam lifetime system was completed at Washington State University.[S. Szpala, M.P. Petkov, K.G. Lynn, to be published (2000)] In the magnetically guided positron beam secondary electrons are collected to generate the time-start signal. The stop is extracted from the detection of one of the annihilation photons. A timing resolution of 350 ± 13 ps at FWHM was achieved. At the expense of timing resolution the signal rate can be increased to accumulate 20 million counts in a spectrum in several hours. This makes depth dependent lifetime measurements on thin films possible. At the best lifetime resolution the lifetime of silicon di-vacancies could be isolated clearly from the bulk silicon lifetime. The performance of the system was examined by

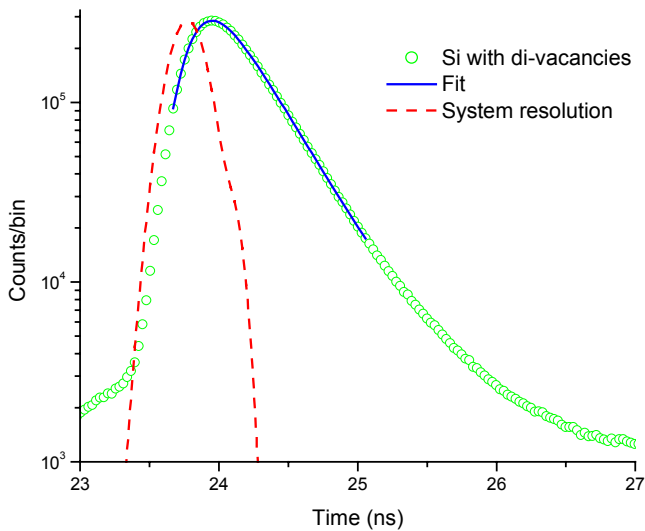


Figure 6 Beam-based positron lifetime spectrum for Si containing di-vacancies. Shown are the raw data (○), the detection system response function (dashed line) and a fit of the response function convoluted with a lifetime spectrum. The fitted resulting lifetime for di-vacancies of 332 ± 7 ps agrees well with previously published results.[P. Mascher 1989]

investigating a sample of Si containing mostly di-vacancies. The data are shown in figure 6 along with the system response function and the result of a fit to the data. The fitted lifetime of 332 ± 2 ps agrees well with the value published earlier by Mascher *et al.*[P. Mascher, S. Dannefaer, D. Kerr, *Phys. Rev. B* **17**, 11764 (1989)]

The angular correlation of the annihilation radiation (ACAR) is a direct complement to the Doppler studies. While Doppler measurements sense the momentum components parallel to the direction of the photon, ACAR measurements measure the small angular deviations from antiparallel photon emission, i.e. the momentum components perpendicular to the direction defined by the sample and the detector(s). Commonly the momentum causing the angular

deviations is measured as an angle. One milliradians equals 0.137 atomic units, which are used in the Doppler broadening measurements. One-dimensional ACAR integrates over one of the two perpendicular directions and 2D-ACAR resolves both. Both methods are valuable tools in the determination of Fermi-surfaces. Recently Tang et al. used the one-dimensional version in combination with positron lifetime data to investigate and confirm the prediction of magic numbers in the size of vacancy aggregates V_n in graphite.[Z. Tang, M. Hasegawa, T. Shimamura, Y. Nagai, T. Chiba, Y. Kawazoe, M. Takenaka, E. Kuramoto, T. Iwata, Phys. Rev. Lett. **82**, 2531

(1999)]. Vacancies and vacancy aggregates are induced by electron and heavy neutron irradiation.

Positron lifetime data are used to extract the fraction of positrons that annihilate in open volume defects and their size. The momentum distribution at the vacancies is separated from the bulk undamaged component and compared to theoretical models for V_n defects. The data are shown in figure 7 for unirradiated, electron irradiated and heavily neutron irradiated graphite. Individual vacancies V_1 result in a bimodal momentum distribution in the c-axis direction at ± 2.1 milliradians (0.288 a.u.), down from 3 milliradians (0.411 a.u.) for defect free graphite. With increasing n in V_n this becomes increasingly symmetric about 0 milliradians. The lifetimes increase from 209 picoseconds for defect-free bulk graphite to 378 ps in V_9 vacancy clusters. The calculations include the shape of the vacancy cluster. Excellent agreement is achieved for V_6 planar rings, which remain stable up to 1500 °C. Figure 8 shows the model calculation results for vacancies and V_6 rings in the hexagonal plane. The asymmetric electron distribution in vacancies becomes symmetric for V_6 . Calculated ACAR data for these systems fit the data for electron irradiated graphite (vacancy case) and heavy neutron irradiation (V_6) very well. The binding energy minimized for the case of V_6 , which explains the “magic size” of a 6 vacancy ring. The bonds in elemental semiconductors like Si and Ge is similar, indicating that such vacancy clusters “magic numbers” may exist there as well.

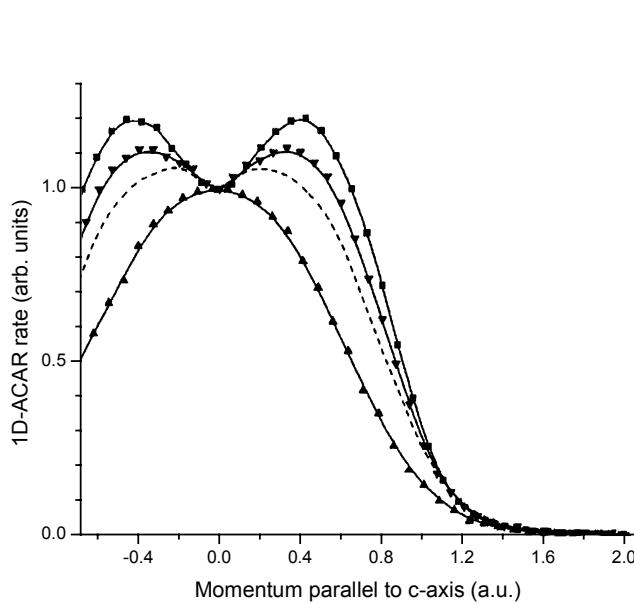


Figure 7 One-dimensional ACAR data for irradiated graphite. The momentum along the c-axis is detected. The bimodal peak distribution of the unirradiated sample (\blacksquare) partially disappears with electron irradiation (θ) and completely with heavy neutron irradiation (π). The defect component of the electron-irradiated data is shown as a dashed line.

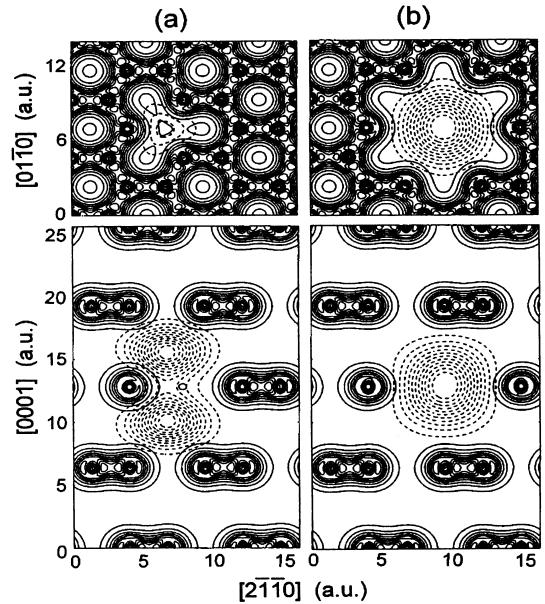


Figure 8 Model calculation for electron (solid lines) and positron densities (dashed) in V_1 (a, left) and planar V_6 rings (b, right). The top figure shows the in hexagonal prism plane and the bottom in the basal plane. The distribution becomes more symmetric in V_6 rings.

A future development will be to combine the lifetime technique with the Doppler-broadening technique. This would allow the separation of positron annihilations at undisturbed lattice sites from those with increasingly larger open volume. This has been demonstrated in a high-energy positron beam age momentum correlation experiment.[W. Weiler, H.E. Schaefer, K. Maier, in “Positron Annihilation”, P. G. Coleman, S. C. Sharma, L. M. Diana, eds. (North Holland 1982),

p. 865] The fast positrons in the beam pass through a thin plastic scintillator to trigger a timing start. The stop is extracted from the positron annihilation event with one of the emerging photons. The difficulty of such a technique is to find an ideal compromise between the need for long time constants to obtain good energy resolution and short time constants for good timing resolution. With this variation of the positron annihilation technique it may be possible to determine the thermal activation energy for mono-vacancies in silicon. The lifetime of positrons in vacancies is larger than that for defect free material. Thus the ratio of positron annihilations in Si vacancies (longer lifetime) to in defect free bulk Si (short lifetime) will increase at increasing times after the positron impinges on the sample and the measurement becomes more sensitive to the defect related events. This has been tried successfully by Suzuki *et al.* on Zn, [N. Suzuki, Y. Nagai, T. Hyodo, Phys. Rev. B **60**, R9893 (1999)] where the activation temperature is larger than it is expected for Si.

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Stress Analysis and Measurement in Si Substrates

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HYDROGEN, PASSIVATION AND RELATED ISSUES

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Abstract

The ability of hydrogen to change the electrical and optical properties of semiconductors has been recognized several decades ago. Experimental and theoretical studies have enormously increased our understanding of H in Si and its ability to passivate defect centers. Yet, the behavior of H is often surprisingly complicated, and many questions are still unresolved. This brief overview summarizes some of the key issues, with emphasis on recent results and open questions.

I. Background

In the 1950s, H₂ was routinely used as (part of) the ambient for crystal growth and/or anneals. It was believed that hydrogen is inert in silicon, just like a noble gas. This is why Van Wieringen and Warmoltz performed their famous experiments[1] of the diffusion and solubility of H, He and Ne. The permeation of these impurities through thin-walled Si cylinders was measured from 1090 to 1200 °C. We now know that the diffusivity they measured, $D_H = 9.4 \times 10^{-3} \exp\{-0.48 \text{ eV}/kT\} \text{ cm}^2/\text{s}$, corresponds not to that of H₂ molecules but of bond-centered hydrogen, probably in the +1 charge state. This diffusivity remains valid down to low temperatures.[2]

In 1957, Fuller and Logan[3] reported that the growth of O-related thermal donors in CZ-Si is greatly enhanced if the material is grown in an H₂ ambient rather than a He ambient. They were the first to notice that special interactions take place between H and O in Si.

It quickly became known that hydrogen improves the electrical and optical properties of Si (and other semiconductors).[4] It was suspected that the formation of Si-H bonds at dangling bonds was the culprit, but direct experimental evidence was lacking and the details of the processes were not understood.

In 1973, Jesse Brewer and co-workers[5] performed muon spin rotation experiments in Si. In addition to the expected Larmor precession of the bare muon (μ^+), they observed *two paramagnetic* forms of muonium (μ^+e^-), a light isotope of hydrogen. ‘Normal’ muonium Mu is atomic-like, but its wavefunction is highly delocalized relative to the free-atom value. But the presence of a second species, which they called ‘anomalous muonium’ Mu*, was totally unexpected. It took some fifteen years[6] before it was identified as bond-centered hydrogen (H_{BC}), hydrogen bridging a Si-Si bond.

The first evidence that H affects the electrical properties of impurities came from studies of ultra-pure Ge used for gamma-ray detectors.[7] This material was grown in a hydrogen ambient to help passivate residual deep traps in the bulk. Hydrogen was found to bind to the electrically inactive substitutional C as well, and the {C, H} pair is a shallow acceptor in Ge. Other impurities in Ge also become activated by hydrogen.

Studies of hydrogen in Si really took off in 1983, when Sah *et al.*[8] reported the passivation (‘deactivation’) by H of the B shallow acceptor. Three years later, Johnson *et al.*[9] reported the passivation (‘neutralization’) of shallow donors.

Since then, a lot of experimental and theoretical work has been done on isolated hydrogen, H₂ molecules, H-impurity and H-defect interactions. Several reviews[4,10] have been published. In the rest of this paper, I will summarize the key information available with emphasis on recent and ongoing research. The paper concludes with a list of unresolved issues and open questions.

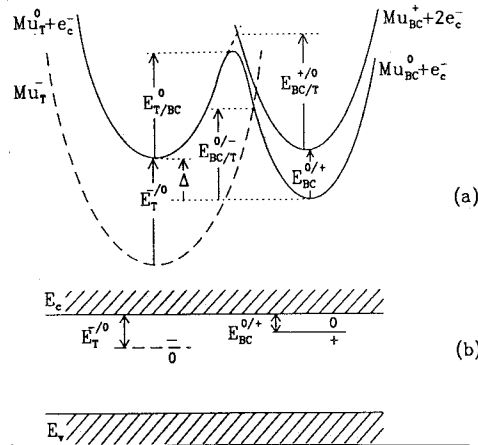
II. Hydrogen in otherwise perfect silicon

Isolated interstitial H exists in three charge states in silicon.[11,12] The positive ion is at a relaxed bond-centered (BC) site, H_{BC}^+ . This is the preferred state of hydrogen in *p*-type Si. The donor level is about 0.2 eV below the conduction band edge.[13,14] The diffusion of H_{BC}^+ occurs by jumps from one BC site to the adjacent one with an activation energy of 0.48 eV as shown by high-temperature *ab-initio* molecular-dynamics (MD) simulations (see e.g. Ref. [15]) or low-temperature reorientation kinetics after stress-alignment.[16]

Neutral (paramagnetic) hydrogen is metastable. Its lowest-energy state has trigonal symmetry at a relaxed BC site (H_{BC}^0), but it also exists at the tetrahedral interstitial (T) site as H_T^0 . The energy difference between the two state is of the order of a few tenths of an eV. The activation energy for diffusion of H_{BC}^0 is virtually the same as that of H_{BC}^+ (the odd electron does not participate in the bonding). However, the barrier for diffusion of H_T^0 along the tetrahedral-hexagonal-tetrahedral path is believed to be much lower.[17] If H_T^0 forms, it diffuses extremely fast[18] until it finds a strained region of the crystal where it traps at a BC site.

The dominant state of hydrogen in *n*-type Si is the negative ion at the T site, H_T^- . This ion is much larger than H_T^0 and its activation energy for diffusion is at least 0.8 eV. There has been much debate[14,19,20] about the position of the acceptor level of H, much of it based on the fact that one must compare the total energies of H_T^- and H_{BC}^0 while only the direct ionization $H_T^- \rightarrow H_T^0$ has been measured (about 0.6 eV). This energy must be corrected by the (unknown) amount $\Delta = E(H_{BC}^0) - E(H_T^0)$ shown in Fig. 1. It is possible that H is a negative-U center in Si, but only by 0.1 or 0.2 eV or so. Above room temperature, there is evidence that several charge states coexist.

Fig. 1: Potential energy diagram for the three charge states of muonium in Si (from Ref.[14]).



In addition to isolated H, two kinds of dimers are observed: the H_2^* complex and interstitial H_2 molecules. The former consists of two Si-H bonds replacing a single Si-Si bond. One H is near the BC site and the other in an anti-bonding position.[21] The two Hs are on the same trigonal axis. This complex anneals out at about 200 °C.

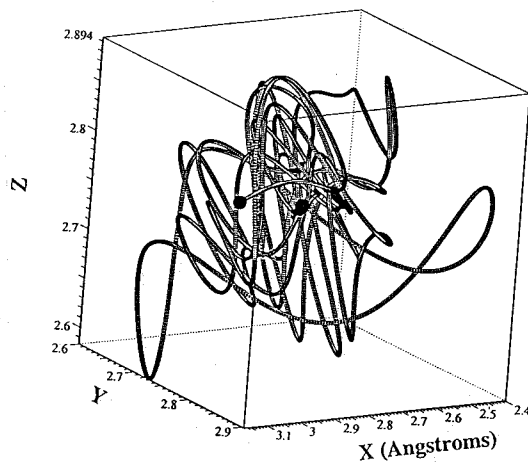
Interstitial H_2 molecules have been seen by Raman[22] and FTIR[23,24] in samples grown in a hydrogen ambient, exposed to a H_2 gas at high temperatures or exposed to a hydrogen plasma. The small and sharp H_2 line is at 3601 cm^{-1} (Raman, room T) or 3618 cm^{-1} (IR, 10 K), substantially lower than that of the free molecule (4161 cm^{-1}).

In oxygen-rich Si samples, three lines associated with H_2 are seen by FTIR[25], two of which are associated with H_2 trapped near interstitial oxygen (O_i). The binding energy of H_2 to O_i is $0.26 \pm 0.02\text{ eV}$ and the activation energy for diffusion of H_2 is $0.78 \pm 0.05\text{ eV}$. Isolated H_2 is seen[26] following anneals up to 350°.

The observed properties of H_2 molecules in Si contrast with all the theoretical predictions published to date (for details, see Ref. [27]). The authors predict that H_2 should be a free rotator at the T site. This implies that the average symmetry should be T_d , the molecule be IR-inactive and the Raman line show an ortho/para splitting, just as it does in GaAs. However, experimentally, the molecule is both Raman[22] and IR[23,24] active and shows no ortho/para splitting. Further, uniaxial stress experiments[28] imply C_1 symmetry, which conflicts with the observation of a single HD line when mixed hydrogen/deuterium gas is used (in C_1 symmetry, HD is different from DH).

Recent *ab-initio* MD simulations[26] show that H_2 does not rotate about its center of mass but instead, the molecule moves within its tetrahedral cage very rapidly, bouncing off the walls, even at temperatures as low as 10 K. The motion of the center of mass of H_2 is shown in Fig. 2. The interactions between the molecule and the crystal provide the (nuclear) spin-flip mechanism needed for H_2 molecules to reach their ground rotational state ($J=0$, para- H_2). Thus, no ortho/para splitting should be seen. The average position of the center of mass moves off the T site at $T > 0$ and shifts when uniaxial stress is applied.

Fig. 2: Motion of the center of mass of H_2 vs. time at 77 K.[28] The T site is at the center of the cube. The nearest Si atom is 2.35 Å away from the center of the cube.



Hydrogen molecules in Si are readily dissociated by electron irradiation[30] or other processes which inject vacancies (Vs) and/or self-interstitials (Is) into the bulk. *Ab-initio* MD simulations[31] show how atomic H is released from interstitial H_2 molecules by Vs and Is. This suggests the possibility of hydrogenating Si during the growth by adding some hydrogen to the ambient. The resulting H_2 molecules would release atomic H following unavoidable processing steps (such as ion implantation or the formation of Al back-contacts) which inject Vs and/or Is into the bulk.

Thus, hydrogen in defect- and impurity-free Si exists as H_{BC}^+ , H_{BC}^0 , H_T^0 , H_T^- , H_2^* , and H_2 . The so-called 'normal' hydrogen diffusion with an activation energy $E_a = 0.48$ eV is that of the BC species. The molecule diffuses much slower, with $E_a = 0.78$ eV, and H_T^- slower still. However, if the metastable state H_T^0 occurs, MD simulations[17] show that it diffuses very much faster than the BC species. DLTS studies[18] of H_{BC} have led Bonde Nielsen and Bech Nielsen to conclude that the diffusivity of hydrogen under their experimental conditions had to be enhanced by 25 orders of magnitude (!) relative to the normal one. They proposed that H_T^0 is the species responsible for this. Other reports of enhanced diffusion[32,33] have been published and various mechanisms proposed, including the diffusion of $\{V, H\}$ pairs[34] and tunneling[35] at low temperatures (quantum tunneling of H in $\{B, H\}$ pairs has been demonstrated[36]).

However, it is likely that some of the reports of enhanced H diffusion are caused by the presence of (invisible) H_2 molecules in the bulk. The rapidly-diffusing species would be either Vs or Is generated at the surface. They dissociate efficiently H_2 , new Si-H bonds form, and hydrogen appears where none was seen before.

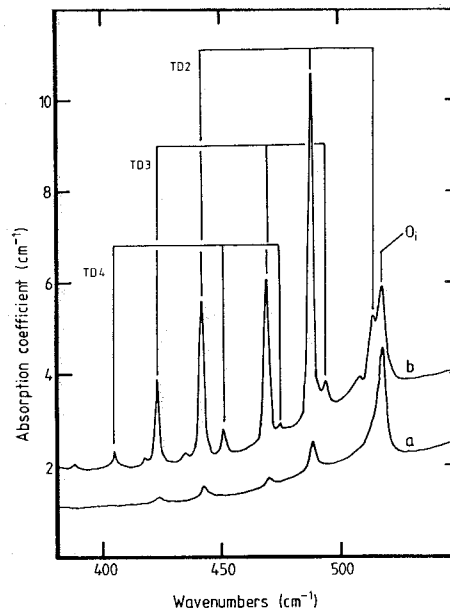
Finally, plasma-hydrogenation often generates disk-shaped platelets, generally in $\{111\}$ planes[33,37]. Platelet formation considerably slows down the hydrogenation and creates defects which act as sites of minority-carrier recombination[38].

III. Hydrogen interactions with impurities

The best-known H-impurity interactions are the passivation of shallow dopants (for a review, see Ref.[10]). In the case of shallow acceptors such as B, the long-ranged attraction between H_{BC}^+ and B^- accounts for the efficiency of the pair formation process. The complex has a three-fold coordinated 'substitutional' B with H tying up the fourth Si bond in a near-BC position. The pair dissociates below 200 °C. In the case of shallow donors such as P, the pair formation is less efficient either because it involves the slow-diffusing H_T^- , or the neutral species H_{BC}^0 and/or H_T^0 which have a much smaller capture cross section by the P^+ ion. When the pair forms, P is three-fold coordinated with a lone pair along the trigonal axis and H weakly binds to the fourth Si atom at the anti-bonding site. The $\{P, H\}$ pair breaks up below 100 °C in the dark and at room T under illumination. The low thermal stability of H-dopant pairs makes them of less interest to the PV community. Note that H also traps at substitutional C, which it activates. But again, the thermal stability is low.

Of greater interest are the interactions between H and interstitial oxygen (O_i). Isolated H (as well as H_2) is attracted to O_i . This is of particular importance in O-rich material, in which H behaves differently than in O-poor Si (say, $< 10^{16} \text{ cm}^{-3}$). The differences are obvious and qualitative when looking at muon spin rotation spectra in CZ- vs. FZ-Si:[39] At low temperatures, all three centers (μ^+ , Mu , and Mu^*) are seen in FZ-Si, but only Mu^* appears in CZ-Si (the fraction of undetected muons is unknown). These spectra are not understood. There is no evidence of a (covalent) interaction between H and O_i . Instead, H acts as a catalyst to enhance the diffusion of O_i , especially in the 300 – 450 °C temperature range.

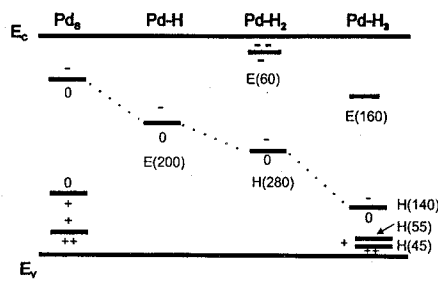
Fig. 3: IR spectra of O-related thermal donors (TDs) in samples annealed at 400°C for two hours in (a) an H_2 gas and (b) a H plasma (from Ref.[40]).



The mechanism of H-enhanced diffusion of O_i has been the subject of several theoretical studies (for a review, see Ref. [17]). Two models have emerged. In the first, H lowers the activation energy for O diffusion by tying up a Si dangling bond at the transition point. In the second, obtained from MD simulations, a covalent H–O pair forms, which transforms the stiff Si–O–Si bridged bond into a H–O–Si bond, with the $\{H, O\}$ pair now able to rotate around the fixed Si atom, allowing it to visit adjacent BC site. This problem is still far from fully understood.

Finally, H also interacts with transition metal (TM) impurities. A number of TM-H complexes have been detected, mostly by DLTS. For example, the trapping of H by Ti, Co, Ag, Pt, Pd, Ni, Cu and other TMs has been reported.[2,41,42] In some cases, equilibrium structures for TM-H complexes have been calculated.[43] However, the DLTS data show that even though H-TM complexes do form, they are not electrically inactive. Hydrogen shifts the position of the TM energy levels within the gap, but no passivation (empty gap) occurs. Further, there is no experimental or theoretical information on the hydrogenation of TM precipitates.

Fig. 4: The evolution of the energy levels of Pt-H complexes shows systematic shifts of several levels, but no passivation (empty gap) is realized (from Ref.[44]).



IV. Hydrogen interactions with native defects

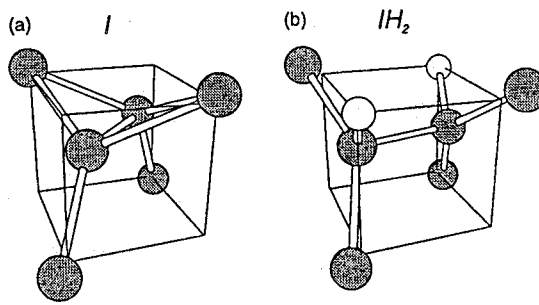
Hydrogen favorite binding site in Si is at dangling or weakly reconstructed bonds such as those found at vacancies (V_s) or clusters of V_s . When H ties up a 'perfect' Si dangling bond, the bond strength is greater than that of a Si-Si bond. As a result, the bonding/antibonding pair associated with Si-H has a doubly occupied eigenvalue in the valence band (bonding) and an empty eigenvalue in the conduction band (antibonding), resulting in the complete passivation of the defect. Of course, the Si bonds at the V and at clusters of V_s undergo some degree of reconstruction and H rarely forms perfect Si-H bonds within the crystal.

The stronger the Si-H bond, the higher the IR-active stretch mode, and the higher the thermal stability. Systematic FTIR studies[45] of H-defect complexes show that H trapped at vacancy-type defects lead to IR bands above $2,000\text{ cm}^{-1}$, the highest frequency ($2,222\text{ cm}^{-1}$) corresponds to the monovacancy saturated with four Hs, a complex which is fully passivated.[46] The calculated binding energies of one H at clusters of n V_s , obtained from $V_n + H_{BC} \rightarrow \{V_n, H\} + \Delta E_n$, give values ranging from 3.0 to 3.8 eV for $n < 4$ and $n > 4$, respectively. The large binding energies suggest that the $\{V_n, H\}$ complexes are thermally stable.

However, theoretical studies[47] of the stability and properties of V aggregates also show that the most stable V aggregates have no deep levels in the gap. The smallest of these aggregates, the ring-hexavacancy V_6 , has only a few empty shallow levels very near the conduction band. This defect has recently been associated with the B_{80}^4 optical center.[48] Thus, some of the V_n aggregates have no (deep) levels in the gap at all. Such centers do trap hydrogen which is expected to activate them. Again, one example is V_6 which, by itself, is almost totally inactive but traps hydrogen and becomes electrically active. Two $\{V_6, H, H\}$ complexes have been identified.[48] They remain stable above 500°C .

Hydrogen also traps at the self-interstitial (I) and, more than likely, at I aggregates I_n . Only one I-H complex has been identified by FTIR and *ab-initio* theory[49], the $\{I, H, H\}$ complex. Its vibrational modes are at 1987 and 1989 cm^{-1} , below those of $\{V_n, H\}$ complexes. Contrary to earlier theoretical predictions[50], it appears that this complex is not passivated by H and that at least four H atoms can trap at a single I[51]. The binding energies are small, ranging from 2.6 eV for $\{I, H, H\}$ down to 1.5 eV for $\{I, H\}$ and just a few tenths of an eV for $\{I, H, H, H\}$. Thus, I-H complexes do form but their thermal stability is low (maybe 200°C or less).

Fig. 5: The neutral self-interstitial (I) (left) and the $\{I,H,H\}$ complex (right) (from Ref.[48]).



V. Challenges

A great deal of information about the behavior of H and specific H-related defects in Si has been obtained in the past ten years from both experiment and theory. Microscopic techniques such as Raman, FTIR, EPR, μ SR, or photoluminescence have allowed the unambiguous identification of the stable states of isolated H and hydrogen dimers as well as numerous defects containing H. These include several H-vacancy and H-self-interstitial complexes or several of the simpler H-TM pairs. As for theory, it is almost always done at the *ab-initio* level (no experimental input into the calculation) in rather larger periodic cells or saturated clusters. A relatively new tool is *an-initio* MD simulations. They are very CPU-intensive but provide the dynamics. The few problems tackled so far with constant-temperature MD simulations show that defect reactions and diffusion can now be studied in real time. As for the problems that are directly relevant to the PV community, some progress has been achieved and new (or rather, more precise) questions have emerged.

The states of isolated H in *n*- and *p*-type Si are known, with still some debate about the negative-U issue. Of the two dimers, H_2^* probably does not play a major role because of its low thermal stability. However, interstitial H_2 may be important. Molecules can be introduced during the growth of the crystal and provide a reservoir in the bulk for atomic hydrogen, to be released by an influx of Vs or Is generated during the processing.

The diffusivity of H_{BC} is well known as is the activation energy for diffusion of H_2 . However, there are many reports of enhanced H diffusion, including tunneling at low temperatures. Although some reports of enhanced H diffusion could be explained instead by the presence of hidden H_2 molecules in the bulk, others cannot. The systematic studies done by A. Rohatgi in the past few years have shown that if a H-rich layer is deposited on the front surface (such as in a nitride grown from an ammonia plasma) and vacancies injected from the back side (during the formation of an Al back-contact for example), a lot of H can be sucked in from the H-rich layer and travel through the entire bulk.

A number of H-impurity and H-defect complexes have been studied. The most stable ones involve perfect dangling bonds which are (almost) permanently passivated following hydrogenation. H also traps readily at V and V_n aggregates with large binding energies. However, only a few of those defects are fully passivated, such as $\{V,H_4\}$. In most cases, the presence of H results in a shift of the defect levels within the gap, but not complete passivation. In some cases, a defect can be activated by H. Hydrogen also traps at I and I_n aggregates, but the resulting bonds are weaker than in the case of $\{V_n,H\}$ and the complexes remain electrically active.

Hydrogen does interact with isolated TM impurities, but DLTS studies show that the resulting complexes remain electrically active. Nothing is known about the interactions involving H and TM precipitates. In fact, the microscopic properties of the TM precipitates themselves is not known. Basic information about TM interactions with O_i , C, V_n aggregates, or other TMs is lacking. The bad regions of a solar cell are known or at least suspected to have TMs trapped in them, but what is it precisely that needs to be passivated (at the atomic level)? Experimental details about the simplest complexes are needed.

Finally, what is so special about H in O-rich Si that renders the behavior of H in CZ material so different from that in FZ material? The H-enhanced diffusion of O_i is just one of the important problems which needs to be understood. Such questions beg for *ab-initio* MD simulations rather than static methods. Theorists still have a lot of work to do.

Acknowledgements

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SIMPLE OECO TECHNOLOGY FOR THE MANUFACTURING OF 20% EFFICIENT LARGE-AREA CRYSTALLINE SILICON SOLAR CELLS

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Abstract: The obliquely evaporated contact (OECO) solar cell structure recently developed at ISFH for the first time allows to reach very high cell efficiencies with an industrially feasible photolithography-free processing. The corresponding fabrication sequence is characterized by four basic manufacturing steps: (i) mechanical surface structuring, (ii) formation of a moderately doped emitter by single diffusion, (iii) contact formation by mask-free oblique vacuum evaporation, and (iv) low-temperature surface passivation by plasma-enhanced chemical vapor deposition (PECVD) of silicon nitride (SiN_x). In this paper, the cell structure and the processing sequence of OECO cells are described together with advantages of this innovative approach. Furthermore, independently confirmed total area efficiencies of 20% and 19.4% are reported for $10 \times 10 \text{ cm}^2$ OECO type solar cells manufactured on boron-doped float-zone silicon and gallium-doped Czochralski silicon, respectively.

1. INTRODUCTION

In order to make solar electricity a large scale economical source of energy, innovative solar cell structures have to be developed combining very high cell efficiencies with simple time- and energy-saving processing. Record laboratory efficiencies of above 24% have been reported in literature for highly sophisticated crystalline silicon solar cells [1]. However, extremely complex processing involving numerous aligned photolithography as well as several high temperature steps were applied. It is evident that due to the large number of complex processing steps, large-scale economic mass production of these cells is not possible.

Avoiding technological limitations and drawbacks associated with the commonly used screen printing or plating, an innovative metallization technology for the manufacturing of large-area high efficiency crystalline silicon solar cells based on obliquely evaporated contacts (OECO) has recently been introduced by our group [2, 3, 4]. As will be shown in this paper the application of the novel mask- and photolithography-free OECO-technology has already led to a number of remarkable results on $2 \times 2 \text{ cm}^2$ laboratory devices as well as on $10 \times 10 \text{ cm}^2$ industrial size solar cells.

2. CELL DESIGN

As an example of OECO-type solar cells, the schematic representation of a highly efficient metal/insulator/semiconductor contacted diffused n^+p junction (MIS- n^+p) device is shown in Fig. 1 (a). The most characteristic features of this unique cell structure are:

- Mechanically formed front surface structure with vertical side-walls for minimized shadowing losses by the front grid and process simplification.
- Moderately doped emitter with excellent quantum efficiency over the whole solar spectrum formed by a single diffusion.
- High-quality metal/insulator/semiconductor (MIS) contacts deposited by mask-free self-aligned oblique vacuum evaporation of aluminum.
- Advanced low-temperature surface passivation by remote plasma-enhanced chemical vapor deposition (RPECVD) of silicon nitride (SiN_x).
- Well passivated rear contact scheme based on local contact areas formed by simple mechanical abrasion.

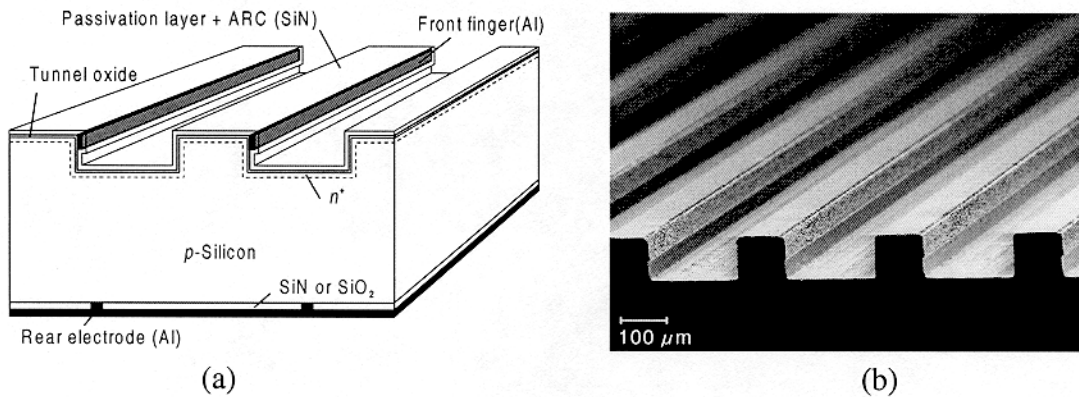


Figure 1: (a) Schematic representation of OECO-MIS- n^+p silicon solar cell characterized by front contacts deposited by mask-free and self-aligned oblique metal evaporation. (b) Scanning electron micrograph of the novel front surface structure with grid fingers formed by oblique vacuum evaporation.

The key feature of OECO cells is their distinct front surface structure providing practically vertical side-walls for the contact formation by oblique vacuum evaporation. Fig. 1 (b) shows a scanning electron micrograph of the novel front surface structure. As can be seen from Fig. 1 (b), the front grid fingers running along the upper parts of the side-walls of the grooves only cause minimum shading. Within this structure the width of the fingers and hence their cross sectional area can easily be adjusted over a wide range by a simple variation of the evaporation angle.

3. PROCESSING SEQUENCE AND MANUFACTURING TECHNOLOGY

The basic fabrication steps of the processing sequence for OECO MIS- n^+p silicon solar cells are depicted in Fig. 2 (a). This processing sequence is especially designed to achieve very high cell efficiencies at an economic cost level in a large-scale industrial environment.

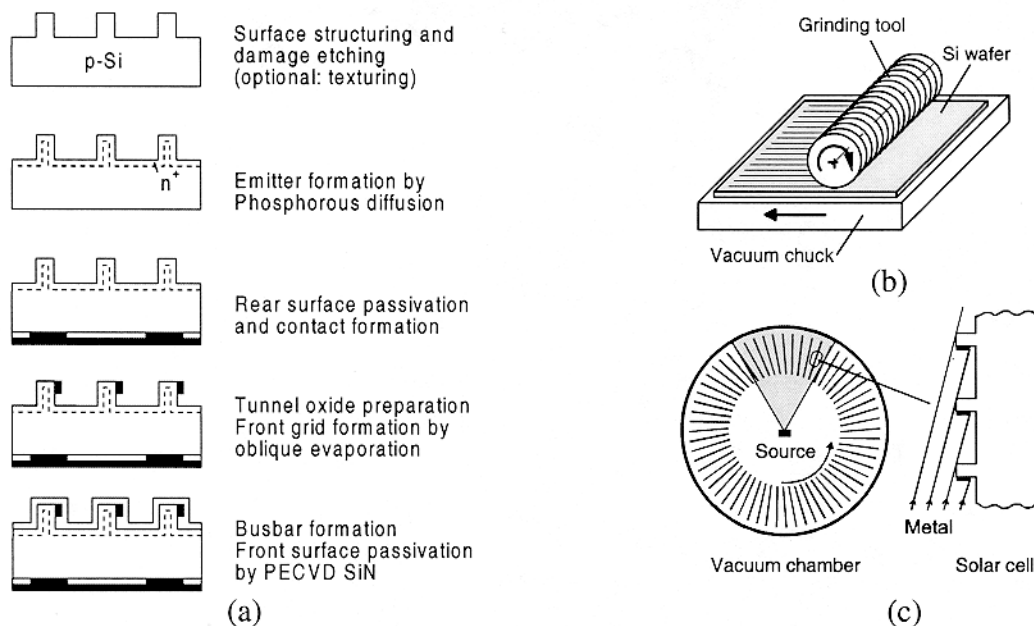


Figure 2: (a) Processing sequence for highly efficient MIS- n^+p silicon solar cells using only aluminum for front and rear electrodes. (b) Schematic representation of custom-made high-throughput grinding system used at ISFH for the formation the front surface structure. (c) Principle of contact formation by mask-free oblique vacuum evaporation.

In a first step the front surface structure consisting of parallel grooves and elevations with steep flanks is formed by mechanical abrasion in a high-throughput grinding system designed to structure silicon wafers up to $150 \times 150 \text{ mm}^2$ in one cut (see Fig. 2 (b)). The grinding is followed by a damage etch which optionally includes surface texturing with random pyramids. After a chemical cleaning an n^+ -emitter is introduced at the front side of the wafer by phosphorus diffusion. Then preferably a low-temperature SiN passivation layer is deposited onto the rear side. Subsequently, the dielectric layer is removed from the rear contact areas by mechanical abrasion and the back metallization is applied [5]. For the formation of the front contacts a tunnel oxide of 1.5 nm thickness is grown and aluminum is deposited onto the steep flanks of the ridge tops by means of oblique vacuum evaporation. As shown in Fig. 2 (c) the self-aligning technique of oblique evaporation is a very simple and reliable method of metallization based on the self-shading effect of the ridges [6]. The busbar interconnecting the grid fingers is formed by simple application of a conductive paste. As a final step, a passivating antireflection (AR) coating consisting of silicon nitride is deposited onto the front of the cell by means of RPECVD.

As to the economy of the oblique evaporation, it can be seen from Fig. 2 (c) that the throughput of wafers can be drastically increased (by at least a factor of 5) compared to the conventional perpendicular vacuum evaporation. The wafers can be arranged closely spaced on a rotating cylinder. As another striking advantage of oblique evaporation nearly all the metal evaporated is effectively utilized. With conventional vacuum evaporation, more than 90% of the metal is lost, and additional processing is required to remove this surplus metal either from shadow masks or from the wafer itself.

4. SOLAR CELL RESULTS

In Table I the measured 1-sun parameters of OECO MIS- n^+p silicon solar cells fabricated at ISFH on boron-doped FZ silicon as well as gallium-doped Cz are summarized. As can clearly be seen from Table I the application of the above-described simple and cost-effective OECO technology has already demonstrated remarkably high cell efficiencies. For industrial-size $10 \times 10 \text{ cm}^2$ OECO solar cells independently confirmed record efficiencies of 20% and 19.4% were achieved using FZ Si and gallium-doped Czochralski silicon, respectively. These values by a clear margin represent the highest efficiencies ever reported for industrially feasible silicon solar cells of this size.

Table I: Measured 1-sun parameters (AM1.5G, 100 mW/cm^2 , 25°C) of OECO MIS- n^+p silicon solar cells fabricated on boron-doped FZ and gallium-doped Cz silicon, respectively.

Material	FZ silicon	FZ silicon	Cz silicon
Cell area	4 cm^2 (aperture)	96 cm^2 (total)	96 cm^2 (total)
$J_{sc} [\text{mA/cm}^2]$	40.5	38.1	37.0
$V_{oc} [\text{mV}]$	666	649	650
Fill factor [%]	78.0	81.1	80.8
Efficiency [%]	21.1*	20.0*	19.4*

* confirmed by Fraunhofer-ISE

5. CONCLUSIONS

This paper highlights the successful application of our innovative OECO technology for the cost-effective manufacturing of highly efficient large-area crystalline silicon solar cells. The simplicity of the novel processing sequence in combination with the outstanding cell results make this approach a promising candidate for a significant cost reduction of solar electricity.

Acknowledgments

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A Review of Back Contact Solar Cells

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Manuscript not available at the time of printing.

Advanced Metallization: From Present to Future

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Introduction

The crystalline silicon solar cell metallization process is still being recognized as one of the most challenging and difficult steps in the manufacturing of cells and modules. At current production volumes, it is difficult to meet standards of reliable processing, while at the same time maintaining cell efficiency.

In the near future, however, an additional challenge arises: thinner and more fragile wafers/sheets will be further exploited to reduce costs, and much larger production volumes are needed to meet demands from the market and use full economy of scale.

This paper surveys developments in metallization and evaluates these against needs of reliability, efficiency and production volume.

Current Metallisation Technologies for Solar Cell Production

Metallization on silicon solar cells is contact formation by deposition and sintering or annealing of conducting material onto the substrate to collect current at the surface. On the deposited metal, strips are soldered to form a series connection of cells into a module. Main requirements for metal contacts are low contact resistance, high conductivity, good mechanical adhesion, and good solderability. Front side contacts need a grid pattern where constraints are focussed on shading loss by the metal coverage, and contact and grid resistance.

Several production methods for contacting solar cells are being used [1,2,3]:

1. Deposition of conductor paste and sintering. This process is typically screen printing of silver and aluminum paste(s) and firing in a belt furnace. This thick film screen print technology is used by almost 90% of crystalline silicon solar cell producers. Advantages are simple and cheap method of deposition with efficient material usage. Disadvantages are relatively high contact resistance, low conductivity of resulting front side silver due to a porous microstructure, sensitivity to thermal load, and low adhesion.
2. Electro(less) plating. Advantages are easy deposition and good conductivity, and insensitivity to anneal temperature and time. Disadvantages are need for masking for line definition (photolithography or laser grooving) and environmental problems associated with disposal of plating solutions. Electroless plating as used in the buried contact technology is considered an affordable (high efficiency) metallization scheme.
3. Metal evaporation and sputtering. Advantages are very good line definition achieved by using masks or photolithography, low contact resistance and insensitivity to anneal temperature and time. A disadvantage is long deposition time to achieve necessary conductance. These methods are used widely for top efficiency cells where cost is not a prime issue.

The reason why screen printing of metal pastes is used so widely has mainly to do with costs, simplicity and ease of automation. This paper will further focus on thick film screen printing technology, as it is the currently prevailing technology.

Thick film technology uses fritted metallic conductor paste, which is deposited onto the silicon surface, dried and then fired to produce electrical contact [4]. Screen printing is the most common deposition method. Other thick film deposition technologies will be discussed later.

Metal paste is deposited with a screen printer using emulsion type screens. Although an established process, it is pushed constantly to practical limits. Advantages of screen print technology are that it is well proven and widely used in solar industries, but also that it benefits from increasing interest of R&D institutes incorporating screen printing in their processing schemes. Disadvantages are that the resulting line definition and conductivity limits cell efficiency, that it is a batch type process limiting process speed, and that optimal transfer of paste is only possible using dedicated equipment, rheologically adjusted pastes, high quality screens and operational craftsmanship.

Deposited paste is dried and fired in belt furnaces to remove organic matter and to form ohmic contact, where an important role is played by glass frit, being the vehicle to achieve proper sintering and contacting. Inadequate firing results in poor cells: too low temperature results in high contact resistance and poor mechanical adhesion, too high temperature gives shunting of the junction. Cell testing is done to characterize the cell parameters. A new method to characterize contact resistance over the full cell surface enabling determination of the cause of bad contacts has developed at ECN [5].

Advances in Metallisation by PV Industry

In the last decade several improvements have been introduced in metallization: fine line thick film screen printing, infra red peak and co-firing, deposition on non-flat substrates, and high speed printing.

1. *Fine line thick film screen printing.* The front side metal coverage is a function of width and number of fingers. For industrial level, the average finger width has been improved from 250 μ m to about 120 to 130 μ m. On pilot line scale however still a factor of two finer finger width has been achieved. Printing of finer and thicker fingers has been realized through advances in screens, pastes, and process control (without reducing the reliability of the process). As a result efficiencies have been increased by about 0.5%. A further decrease in line width without change in the process seems to lead to a reduction in process reliability. Screens have to be cleaned more often, and more fingers will contain interruptions. Interest to go finer is still there; limitations are, however, formed by paste rheology [6,7].
2. *IR peak and co-firing.* The last decade showed a transition from resistance type to infra red heated furnaces. IR firing, which allows for spike firing with fast ramp rates together with a short peak temperature dwell time, has become a standard. Due to glass frit, good contacts can be achieved in an IR furnace at high temperature and during a short time interval. Co-firing front and rear side has been introduced and is widely applied. The IR process also opened possibilities for firing on or through more delicate surfaces, like the TiO_x or SiN_y anti-reflective coatings and also onto shallow emitters [8,9]. However, firing needs to be carefully optimized for particular paste used, in view of the absence of pastes with a wide processing window.
3. *High-speed printing.* Due to the lack of dedicated solar screen printers, generally equipment of hybrid circuit manufacturing industry has been preferred. As a result of collaboration in a European project, EKRA recently came out with a dedicated solar screen printer with a throughput of 1200 cells per hour. Further increase of throughput seems possible. Commercial screen printers for other substrates are available with a throughput of up to 2,500

substrates/hour. With high throughputs, handling and further transport of wafers becomes an important issue.

4. *Deposition on non-flat substrates.* For non-flat, sheet type materials, contact technology of screen printing cannot be used without adaptations. One approach used industrially is (off-contact) direct writing method that transfers paste to the substrate using a way of dispensing [10]. Another applied method uses pre-fabricated decals that are applied on the cell and fired to make the contact [11]. Both methods are patented and similar developments by others have not been reported.

Advances in Metallisation by R&D Institutes

Research on metallization processes by R&D institutes has focussed on achieving high efficiencies, implementation of new cell concepts and introduction of advanced equipment and materials. The main aspects are summarized as follows:

1. *High efficiencies:* By IR firing through SiN and onto shallow emitters high efficiencies are reached [12,13] and these technologies are finding their way to industry. To speed up processing rapid thermal processing (RTP) is being researched [14] and RTP firing or annealing shows promising results [15]. Higher ramp rates of RTP can be controlled with more freedom and much more precisely, so that a small process window does not necessarily mean a less reliable process. RTP is however a slow batch type process, but developments aim at semi-continuous RTP furnaces [15].
2. *Improved printer technologies.* For new concepts like EWT, PUM and MWT back contact cells, for cells with mechanical texturization and cells with selective emitters, more precise (interdigitated) printing is necessary. On R&D scale, printers manufactured by Baccini and EKRA have accomplished this. Automated wafer alignment and print positioning is also feasible at 1,200 cells/hour or more.
3. *New mask materials.* A disadvantage of screens is that mesh material, necessary to keep the pattern together, is an obstruction for optimal paste transfer and release. Therefore finer fingers with a high aspect ratio cannot be reached reliably with current materials. Higher quality stainless steel mesh, new mesh material, or differently built up screens, all resulting in larger open areas, have become available and are being tested [16]. A different approach is application of metal stencils [3]. Stencils can now be produced with beneficial characteristics. Non-wear character of electroformed nickel material allows for a higher number of prints and constant print quality. Much larger open area and better release properties allow for fine and high line printing [17,18]. Stencil printing is being tested under manufacturing conditions [19].
4. *New deposition methods.* A limitation of flat bed screen printer technology is that it is a batch type process. This has a drawback on total cycle time, where print speed is only one issue. To accomplish higher throughputs research is being carried out on rotation type printing methods like roller printing, off set gravure printing and rotational screen printing [20,21]. Advantages are that these are fast and continuous processes, where wafer transport can be simplified. In rotational printing, paste is continuously being sheared and roller printing has advantages for depositing paste onto mechanically texturized wafers. Multi-step fine line pad printing for higher efficiency is also under development. All methods are, however, not available for industrial application yet.
5. *Paste rheology and chemistry.* So far paste manufacturers do know how to make pastes, but they claim to have had inadequate feedback of results obtained by R&D and cell manufacturers. Paste suppliers generally have insufficient knowledge of how to make a solar

cell, whereas R&D and manufacturers who know how to make a cell typically do not know about all important aspects of the pastes. This has changed during recent years. For instance, the paste manufacturer ESL has installed a cell tester to evaluate the relation between paste characteristics and cell results. This has resulted in a new front side paste that was well received. A cooperation between Ferro and GeorgiaTec led to more insight in firing and paste composition [22]. Little is still known, however, of chemical/physical processes that occur during formation of the metal silicon interface as a function of glass frit composition. Only during the last few years R&D institutes have started their own research on this issue [23,3]. Paste modification has been utilized for improving contacting behavior [24]. Tentative schemes for interface reactions have been proposed [25,26]. At ECN new pastes were developed, where emphasis was not only on compositional influence for realization of the contact, but also on rheological aspects to enable high aspect ratio fine line printing [27,19]. Also work has been performed on the modification of pastes for combining process steps, like boron doping of aluminum paste for BSF enhancement [28] and Ag antimony doping for low contact resistance and self doping [29].

What R&D on Metallization is Necessary for Future Production?

Production of solar systems is driven by cost of produced energy in \$/kWh. On cell/module level this cost is a result of efficiency, process reliability, and volumes. Any advancement in metallisation should take these factors into account as well. For high volume production, reliability issues become even more important, putting their constraints on high efficiency processes.

The following trends are observed in the industry:

1. *Application of thin wafers.* In order to reduce costs the trend is towards thin wafers. Metallization of these wafers, however, may lead to a lower yield, mainly due to more breakage. Another problem is bending of wafers due to the use of full coverage aluminum back contacts. New ways of passivating the rear surface are currently being researched at R&D institutes [30]. Metallization on these surfaces is not likely to present a problem.
2. *Increase in non-flat substrates.* There is more interest in producing cheaper crystalline silicon wafers/sheets. Deposition techniques for these non-flat wafers have already been discussed. Since these techniques are assumed to be less reliable and slower than screen printing, other (e.g. off-contact, easy transfer, low pressure) deposition techniques, need to be introduced by R&D institutes. Best candidates are stencil printing, off-set and dispensing.
3. *Integration of high efficiency processes into production.* Several new or improved processes for production of high efficiency cells have been introduced by R&D institutes. Two of these will be discussed here with respect to research on metallisation.
 - Texturization. Due to different morphology these substrates are more difficult to print on. This will lead to more coverage by paste spreading and increased contact resistance. Adequate printing using paste with optimized rheology will have to be demonstrated. Another solution is the use of non textured plateaus, which dictates alignment of the metallization. This is demonstrated on lab scale using dedicated equipment.
 - Shallow emitters with SiN. This approach has been shown on lab scale to be beneficial. However, the process window is narrowed down, because shorting the emitter is more likely. This makes the introduction to industrial application more difficult. Research should aim at widening the process window through improvements to the chemical composition of the paste and better control of the firing process for instance by the implementation of continuous RTP.

4. *High reliability metallisation.*

- New masks need to be introduced in production. Stencils together with pastes with adapted rheology must find their way to pilot scale production for testing on large numbers of substrates.
- A wide process window must be available even for standard solar cell manufacturing. To achieve this, paste characteristics need to be optimized and be guaranteed for constant quality.

5. *High volume production.* To fully benefit from economy of scale larger production volumes are needed. Increasing higher throughputs relates more to the process of screen printing than firing. Options regarding to higher volumes are:

- Use more printers: This approach will not lead to cost reduction.
- Use higher throughput processes by speeding up and finding optimum cycle time, and/or by introducing printing on more than one substrate. This can be achieved by R&D assisted engineering of these printers.
- Use new printing processes: move from batch type to continuous type rotational printing. Role of R&D is to develop these technologies.

Conclusions

With emphasis on thick film metallization, an overview has been given of the technologies used in industry and researched at R&D institutes. The following conclusions are made:

1. Deposition and firing of metal pastes is the most widely used technology for crystalline silicon solar cell metallization and will be further exploited, because of its simplicity and low operating costs. A disadvantage is that it is difficult to reach high efficiencies, because the process is sensitive and dependent on operational factors and non-optimized materials.
2. Interest and emphasis of the industry is mainly aimed at improving reliability of the process and increasing production volumes. Achieving higher efficiency should not interfere with process reliability: i.e. industry is conservative in adapting improvements from R&D institutes.
3. R&D institutes are mainly aiming at reaching highest efficiencies. Effort should focus more on widening process windows and increasing process reliability to enable easy transfer to industry.
4. Issues that need to be addressed to achieve cost-effective, ten-fold increases in production volumes from current levels, while maintaining efficiency, include:
 - Advanced deposition technologies for flat and non-flat substrates. To fully profit of economies of scale, a change towards rotational print or continuous off-contact techniques is necessary.
 - Improved materials with guaranteed constant quality, which allow reliable high efficiency processing with a wide processing window:
 - Masks and pastes, with improved rheology, for fast printing of fine line high aspect ratio front side contacts.
 - Pastes with improved glass frit composition for wider process windows in high efficiency scenarios such as firing through passivating coatings on shallow emitters.

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Conductive Adhesive Joining Technology In Electronic Packaging

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In electronic packaging applications, tin-solders, due to their toxicity and environmental incompatibility, are being replaced by conductive adhesives. Although there have been much progress in applications of conductive adhesives, the electronic packaging industry itself is still in its infancy. It is hard to find a single conductive adhesive that will meet demanding expectations of both electrical and mechanical performances. In this talk, a brief review of the application of conductive adhesive technology is given. Following, we focus our attention back to some of more fundamental issues such as topology of contact connectivity among filler particulate material. In order to accomplish this, we employ a discrete particle simulation. This method is capable of taking into account dynamics of interacting particles in epoxy. However, we will demonstrate our capabilities by presenting some intriguing physics found in compacting dry filler particles. We will present results from our analyses based on spherical particles and elliptical particles both with/without size distributions. Conductivity (or connectivity) will finally be summarized in terms of size, shape, number of contacts and the resistance defined by connectivity chains.

MONOLITHIC MODULES WITH PRINTED INTERCONNECT PATTERNS

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ABSTRACT: As a complement to Evergreen Solar's use of continuous Si ribbon growth (String Ribbon) and polymeric materials for PV modules, a method is described whereby cells with wraparound contacts are interconnected in a monolithic fashion using conductive interconnect patterns printed on the backskin. A significant reduction in processing steps and cost can be realized by this technique, and thinner Si ribbon can be processed with higher yields. Modules with 84 cm² and 120 cm² String Ribbon wraparound cells were formed using this monolithic module procedure. Accelerated reliability testing of these modules is encouraging.

1. CONVENTIONAL VS MONOLITHIC INTERCONNECT STRUCTURES

In an effort to lower costs in all steps of manufacturing photovoltaic modules, Evergreen Solar has developed a method for the continuous production of silicon ribbon directly from the melt [1] and novel polymeric materials to replace the conventional materials now used as an encapsulant [2] and as a backskin [3]. In this work, a low-cost method to interconnect cells with wraparound contacts has been developed wherein the interconnect patterns are formed by printing conductive inks upon the backskin.

The conventional technique used by industry to interconnect single crystal or multicrystalline Si solar cells involves the soldering of flat wires from busbars on the front of the cells to contacts on the backs of the cells (see Fig. 1a).

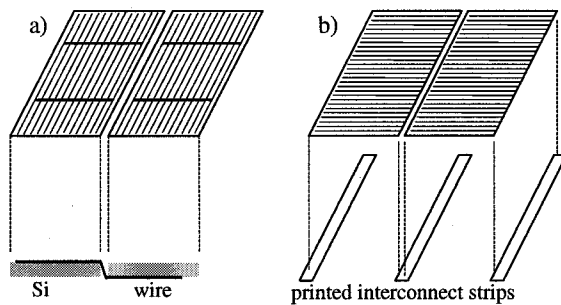


Figure 1: Cell interconnection techniques for a) conventional silicon wafer cells, b) Evergreen Solar's monolithic interconnects for silicon wafers.

An example of conventional module assembly production flow is shown in Figure 2. This technique has several disadvantages:

- The cells experience excessive handling and thermal shock which can lead to yield loss in terms of cell breakage.
- The handling of already soldered strings is difficult and can lead to broken solder bonds.
- The equipment used to automate these processes is expensive and difficult to maintain, or alternatively, the labor costs for unautomated processes are high.

- Front busbars block light and are considered aesthetically unattractive for some architectural applications

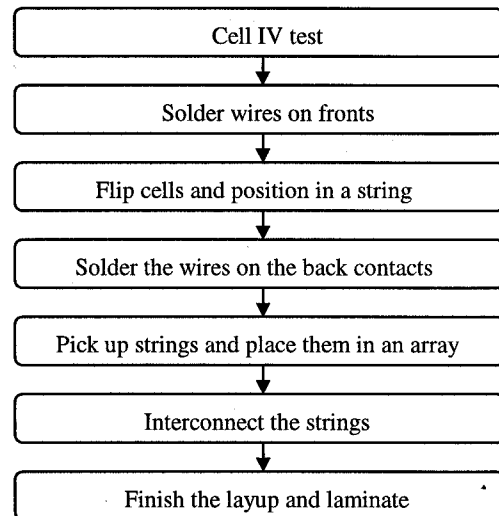


Figure 2: Module assembly production flow using the standard interconnect structure.

Instead, we would prefer a simpler process with fewer cell handling steps. As an alternative, some PV technologies use processes that create so-called *monolithic* interconnects. This term implies that the connections between cells form as a consequence of processing steps applied to the whole module structure as opposed to the case here where cells are connected one by one and then are placed onto the module structure. In this paper we present a type of simple monolithic interconnect structure (see Fig. 1b) wherein all interconnections between cells occur on the back side of the cells.

2. WRAPAROUND CELLS

Several groups have worked on back contact silicon cells. Many have used *wrapthrough* structures where an array of holes are laser cut, sawed, or etched through the wafer, and later the emitter and/or front contacts are wrapped through the holes to the back side. [4-10]. However, such processes do not match our low-cost goals since they involve a large number of processing steps, and since we wish to completely eliminate any silicon etching. Other groups have worked on back junction cells [11,12], but such cells

require silicon with minority carrier diffusion lengths greater than the cell thickness and again require complicated processing steps. Still others have worked on *wraparound* cells where the emitter contacts wrap around one or more edges of the cell to the back surface [5,13].

In order to minimize the number of processing steps applied to the wafers, Evergreen Solar has developed a transfer method whereby the Ag and Al contacts are remotely printed and dried in separate steps. These patterns are then applied to the wafers in a gentle manner with low yield loss, even with thin wafers. In addition, any yield or quality problems with the printing steps are effectively decoupled from the cell yield, and large screens may be used for exceptional throughput. This indirect printing method is well suited to wraparound cell fabrication, since the dried Ag emitter metallization paste is somewhat flexible in its green state.

The front side of an 8.0-cm wide cell is shown in Figure 3. Most of the back side is covered by Al paste. These cell metallization patterns are currently transferred by hand to the wafers, but in future work we will automate the pattern transfer step.

The performance of cells with Si_3N_4 antireflection coatings are shown in the table below. With the limited work performed to date, wraparound cell efficiencies have been somewhat lower than those for conventional String Ribbon cells. With further development, particularly in the area of reducing shunt conductance, we expect this difference to narrow significantly.

Table I. Performance of 15x8 cm wraparound cells.

AR	Voc	Jsc	FF	Eff.
TiO_2	0.546	28.4	66.4	10.3
Si_3N_4	0.579	29.3	67.4	11.4

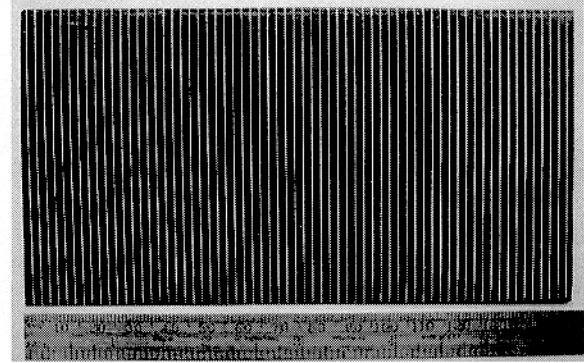


Figure 3: Front side of a 15 x 8 cm wraparound cell.

3. MONOLITHIC MODULES

The proposed production flow for monolithic modules is shown in Figure 4. As compared to the production of standard modules using cells sawed from ingots, the number of processing steps and the cost are significantly reduced. In comparison to the conventional tabbing and stringing procedures shown in Figure 2, the module layout segment of the operation is greatly simplified.

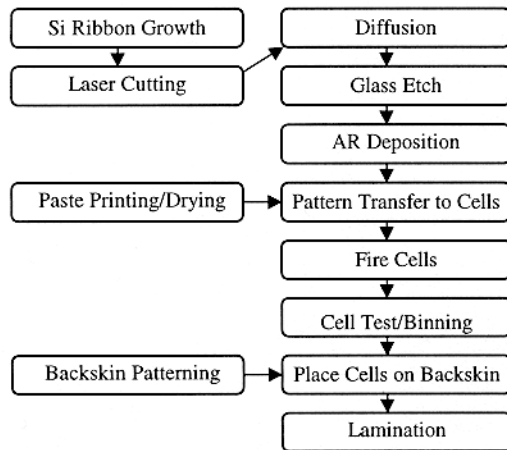


Figure 4: Future production flow for monolithic modules.

In the single wrap structure, the current needs only to travel a few mm's in the interconnect metallization as opposed to several cm's in the double wrap structure. Thus, the conductivity requirements of the pattern are greatly reduced. In addition, a much smaller total area of interconnect metallization is needed, and wrapping the transfer pattern around one edge of the cell is easier than wrapping it around two edges.

Assume we have cells of width W (8 cm) with a maximum power point at a current density J_{max} (27 mA/cm²) and voltage V_{max} (0.58V). In addition we have a spacing d (1.6mm) between cells, and an interconnect strip with bulk resistivity ρ and thickness

We considered two different interconnect patterns (see Figure 5), depending on whether the fingers wrap around one or two edges of the cell. The double wrap approach has the advantage in that fewer fingers are needed on the front side (less shadowing loss) since the I^2R power losses in the Ag are less, but the advantages and elegance of the single wrap approach are overwhelming. This pattern is similar to the one proposed by Gee for interconnecting *emitter wrap through* cells in his vision of *monolithic module assembly* [14].

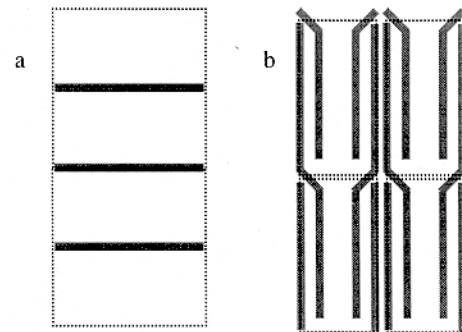


Figure 5: Interconnection pattern for cells with a) single and b) double wrap patterns.

t. Assuming a low contact resistance between the cell metallization and the strip, the power loss due to current travelling between adjacent cells can be approximated by:

$$\%P_{loss} = 100 \cdot \frac{J_{max} W d \rho}{V_{max} t} \quad (1)$$

This is plotted in Figure 6:

:

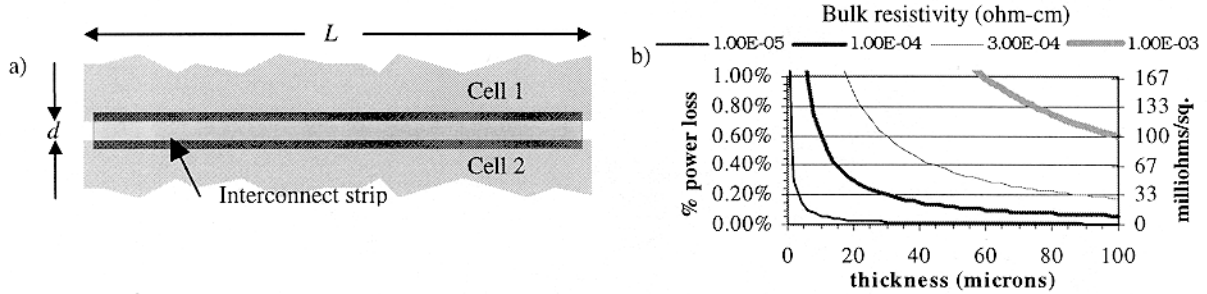


Figure 6: a) Schematic of the interconnect structure between single-wrap cells, and b) a graph of % power loss for interconnect strips with different bulk resistivity and thickness.

The properties of Evergreen's novel backskin material allowed for several possibilities of accomplishing the interconnection process. Metal foil strips can be directly bonded to the backskin, or a conductive material can be printed directly onto the backskin. With a sufficiently large printer, all the patterns in a module may be printed in one step, thus ensuring perfect alignment between successive interconnect strips. Several different conductive materials were evaluated in terms of their conductivity, the contact resistance with fired Ag/Al or Ag paste on the cells, and in terms of the performance of modules or minimodules constructed with these materials under accelerated testing.

A module usually contains more than one column of cells. The connections between these columns is usually established with wide pieces of Sn or solder-coated Cu ribbon. In these interconnect pieces, the current travels along the length of the structure, not across the short width dimension, so the conductivity requirements are much higher than for the connections between cells. We used Cu ribbon strips for these interconnections in the prototype modules and minimodules.

Following cell testing, a vision guided robot can merely pick up the cells and place them on the patterned backskin. The backskin itself is a modified thermoplastic which strongly bonds to the backs of the cells during the lamination cycle, thus eliminating the need for an encapsulant layer between the cells and backskin. Frameless modules have also been made using this material [15]. After the cells are placed on the backskin, the external contact leads are incorporated, and a sheet of Evergreen's novel encapsulant and the coverglass are placed on top. The entire structure is then placed in a laminator. Photos of standard and monolithic frameless modules using 84-cm² cells are shown in Figure 7.

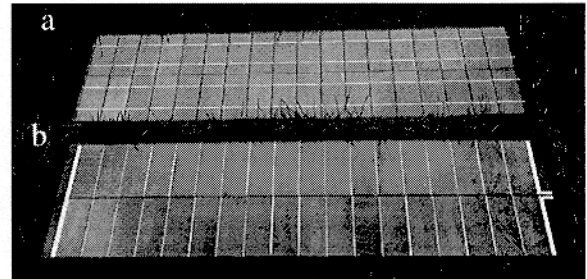


Figure 7: Frameless modules with a) standard and b) monolithic interconnects.

We placed small modules in a humidity/freeze chamber and exposed them to accelerated testing where one 24 hour cycle comprised at least 30 minutes at -40°C and 20 hours at 85°C with 85% relative humidity. As is shown in Figure 8a, the relative output power reduction of the module is less than 0.5% after 100 such cycles, indicating good module stability. We also exposed larger modules to 100 purely thermal cycles. One 4 hour cycle goes from -40 to 90°C and back down. Good stability was also seen for these modules as is shown in Figure 8b. All of the module testing was performed on modules made with the previous generation of 5.6-cm wide cells with TiO₂ antireflective coatings. We will expose modules with 8-cm wide, Si₃N₄-coated cells to larger numbers of cycles and other reliability tests in future work.

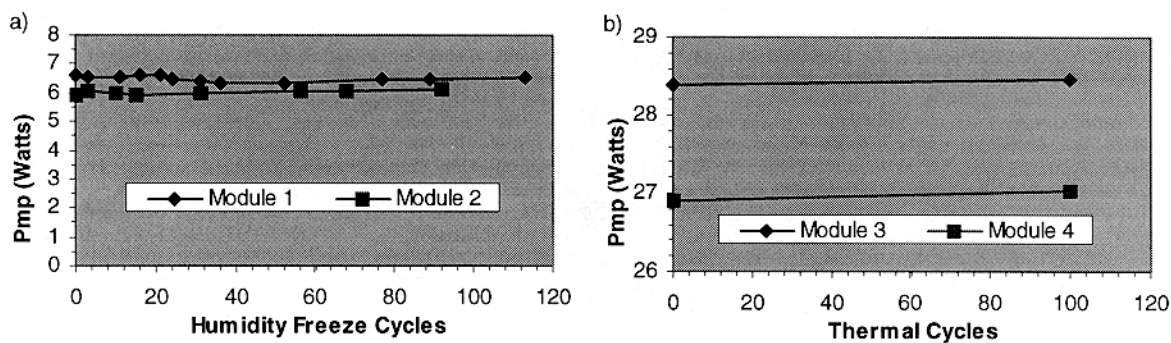


Figure 8: Monolithic module performance under accelerated a) humidity/freeze and b) thermal cycling.

4. CONCLUSIONS

We have demonstrated a module manufacturing process with a greatly reduced number of processing steps as compared to conventional module processing. In particular, several steps that involve handling of the wafers have been eliminated. Evergreen's goal is to shift production toward 100- μ m ribbon. The reduction in processing steps will facilitate the transition toward thinner wafers in the future where the sensitivity to yield loss from handling wafers is increased. Many of the problems in fabricating cells with wraparound contacts have been addressed, but more work is needed to bring cell efficiencies up to the level of standard cells, particularly in the area of reducing shunt conductance. These wraparound cells were successfully connected by a conductive interconnection pattern printed on the module backskin. Module reliability tests show promise for this monolithic interconnect structure.

5. ACKNOWLEDGEMENTS

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**Low-Cost Crystalline Silicon Wafers and Foils for Solar Cell (KOSI):
A New German Research Program**

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Rapid Crystallization of Silicon Thin Films and Its Device Application

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Fundamental properties of laser crystallized polycrystalline silicon films are discussed. Laser rapid crystallization resulted in small crystalline grains < 100 nm. Analyses of free carrier optical absorption revealed that crystalline grains had excellent electrical properties with a high carrier mobility, while grain boundaries were a high carrier scattering region resulting in low electrical current traversing grain boundaries. The reduction of density of defect states was demonstrated by heat treatments with oxygen plasma and with high-pressure H_2O vapor annealing at low temperatures $< 300^\circ\text{C}$. These heat treatments realized increase in the carrier mobility to from 87 to $160\text{ cm}^2/\text{Vs}$ and decrease in the threshold voltage 3.8 to 1.3 V for the polycrystalline silicon thin film transistors. Rapid crystallization using the electrical current induced joule heating method was also presented for formation crystalline films with a grain size larger than $10\text{ }\mu\text{m}$.

1. Introduction

Polycrystalline silicon films have been applied to many devices such as thin film transistors (TFTs) and solar cells. Many technologies have been reported for formation of polycrystalline silicon films at low processing temperatures [1-6]. Pulsed laser crystallization method has an advantage for formation high-quality polycrystalline silicon films via rapid melting followed by solidification. That method has been therefore applied to fabrication of poly-Si TFTs and its electronic circuits.

In this paper, we first discuss fundamental properties of rapid laser induced crystallization of thin silicon films. We report structural and electrical properties of polycrystalline films. We analyze electrical conductivity of polycrystalline silicon films, which strongly depends on properties of grain boundaries. We present passivation of grain boundaries of laser crystallized silicon films by oxygen plasma treatment and high-pressure H_2O vapor annealing. We apply these methods to fabricate poly-Si TFTs with high performances. We finally present another rapid crystallization method with electrical-current induced joule heating of silicon films in order to fabricate large crystalline grains.

2. Pulsed laser crystallization

Crystallization of silicon thin films formed on quartz glass substrates occurs when silicon films are heated by 30-ns-pulsed XeCl excimer laser with a wavelength of 308 nm and a laser energy density above $160\text{ mJ}/\text{cm}^2$. The silicon films are rapidly melted by laser irradiation. Crystallization occurs according to solidification of liquid silicon after laser irradiation. The liquid/solid interface moves toward the surface

according to heat diffusion into the substrate. The speed of the interface was experimentally determined as about 0.6 m/s by measurement of change in the electrical conductance of liquid silicon [7]. Crystalline grains can grow spherically from nucleation sites located near the Si/quartz interface in the initial stage of melting (interface controlled growth). The grain growth is limited by the film thickness and the melt duration. The crystalline grain size increases as the laser energy increases. When the silicon films are melted almost completely, lateral grain growth occurs. Rapid crystalline growth has been observed in the lateral direction about $1\text{ }\mu\text{m}$. [8]. On the other hand, amorphization occurs when the silicon films are melted completely by laser irradiation with a high energy density. very rapid solidification to amorphous or microcrystalline states occurs [9]. Complete melting of silicon films on a glassy quartz substrate results in a super cooling state. Very rapid solidification with a high liquid/solid interface velocity is realized because the free energy in liquid silicon in a deep super cooled state is much larger than solid silicon at the solidification temperature. The latent heat energy per unit area released at solidification determines solidification temperature. Films thicker than 30 nm are solidified to microcrystalline states because large latent heat energy increases the solidification temperature. On the other hand, films thinner than 30 nm are amorphized after solidification.

Measurement of Raman scattering spectra gives evolution of crystalline states of laser crystallized films. The spectra of initial amorphous films had a broad peak around 450 cm^{-1} . A small and sharp peak associated with the transverse optical (TO) phonon of crystalline silicon appeared in the spectrum for the sample heated at the crystallization threshold of $160\text{ mJ}/\text{cm}^2$ [10]. The crystalline TO phonon intensity increased and the intensity amorphous TO phonon peak decreased to

almost zero as the laser energy density increased. The crystalline volume fraction was about 0.4 for laser irradiation at the crystallization threshold. A high energy density of 360 mJ/cm^2 , much higher the crystallization threshold, was required to achieve a crystalline volume fraction almost one [10].

An analysis of optical reflectivity spectra of doped silicon films gives the average carrier mobility and the carrier density in crystalline grains because free carrier optical absorption occurs via excitation induced by the electrical field of incident photons followed by energy relaxation in the crystalline grains [11,12]. On the other hand, the Hall effect current measurement provides the effective carrier mobility of the electrical current, which traverses many grain boundaries in polycrystalline silicon films, so it strongly depends on grain boundary properties. We developed an analysis program of free carrier optical absorption for multiple silicon layered structure on glass substrate including optical interference effect in order to estimate the carrier mobility and the carrier density in the crystalline grains. Using the program, we calculated the optical reflectivity spectra with carrier mobility and carrier density as parameters and fitted to experimental spectra measured in the infrared region between 400 and 4000 cm^{-1} using a conventional Fourier transform infrared spectrometry (FTIR).

Figure 1 shows the carrier mobility obtained by the analyses of free carrier absorption and by Hall effect measurements as a function of laser energy density for 50-nm thick silicon films doped with $2.5 \times 10^{20} \text{ cm}^{-3}$ phosphorus atoms. Samples were crystallized by laser irradiation with increasing the laser energy density step by step with single and 5 pulses at each energy density step. Dopant atoms were activated and a high density of carriers was generated. The analysis of free carrier absorption gave a large carrier mobility about $20 \text{ cm}^2/\text{Vs}$ for samples annealed at 160 mJ/cm^2 , crystallization threshold, although the average grain size was small, about 10 nm as obtained by TEM measurements. The carrier mobility increased to $40 \text{ cm}^2/\text{Vs}$ as the laser energy density increased. Irradiation with a single pulse and five pulses for each energy density step resulted in approximately the same carrier mobility. These results indicate that laser irradiation formed crystalline grains with good electrical characteristics even for lower energy densities near the crystallization threshold energy. The maximum carrier mobility of $40 \text{ cm}^2/\text{Vs}$ obtained by analysis of free carrier optical absorption was close to that of single crystalline doped silicon reported by Irvin [13]. This means that the crystalline grains formed by the laser crystallization method have approximately the same electrical properties as single crystalline silicon. The Hall effect measurements resulted in lower carrier mobility than those obtained by the free carrier optical

absorption analysis. The carrier mobility obtained by the Hall effect measurements markedly increased from $3 \text{ cm}^2/\text{Vs}$ to $28 \text{ cm}^2/\text{Vs}$ as the laser energy density was increased. This increase is interpreted as improvement of the grain boundary properties by laser irradiation with high energy densities. Disordered states with a high carrier scattering rate at the grain boundary were reduced by laser irradiation with high energy densities because of the long melt duration and the low quenching rate. Moreover, the carrier mobility obtained by Hall effect measurements for samples crystallized with 5 pulses was higher than that for samples crystallized with a single pulse for high laser energies of $310 \text{ mJ/cm}^2 \sim 375 \text{ mJ/cm}^2$. Multiple pulse irradiation is important for reduction of the average barrier height at grain boundaries.

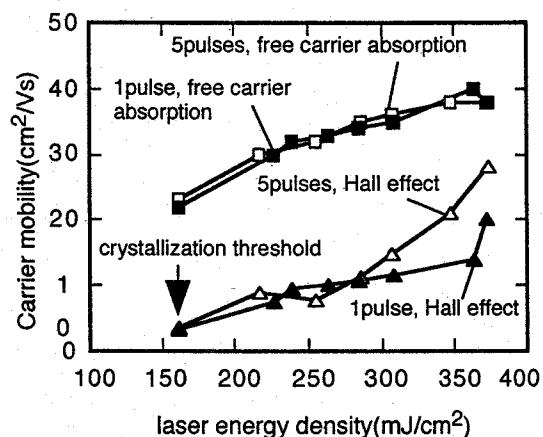


Fig. 1 Carrier mobility obtained by analyses of free carrier absorption and by Hall effect measurements as functions of the laser energy density. The samples were $2.5 \times 10^{20} \text{ cm}^{-3}$ phosphorus doped 50-nm thick silicon films.

Figure 2 shows the carrier mobility as a function of temperature for 50-nm-thick phosphorus doped silicon films crystallized at 160 mJ/cm^2 and 280 mJ/cm^2 . The carrier mobility obtained by the analysis of free carrier optical absorption increased monotonously as the temperature decreased from 473 K to 77 K for both samples. The mobility increase is interpreted as reduction of carrier scattering caused by the lattice vibration. On the other hand, the Hall effect measurements revealed that the mobility slightly decreased as the temperature decreased from 473 K to 77 K for the sample crystallized at 160 mJ/cm^2 , while the polycrystalline silicon films formed at 280 mJ/cm^2 showed little temperature dependence of the mobility. The grain boundary properties in the low laser energy

case were poor and the thermal excitation energy was required for carriers to go across the boundaries.

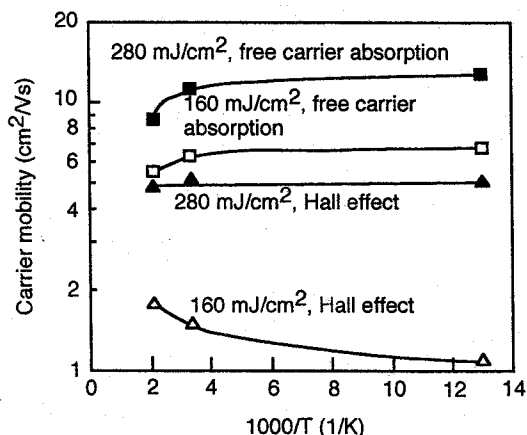


Fig. 2 Carrier mobility obtained by analyses of free carrier absorption and by Hall effect measurements as functions of temperature. 50-nm thick phosphorus-doped silicon films were crystallized by laser irradiation at 160 mJ/cm² and 280 mJ/cm². The carrier density was about 2×10^{21} cm⁻³ for both samples.

3. Improvement of electrical properties of poly-Si films

Observation of transmission electron microscopy (TEM) [7] and analyses of free carrier optical absorption and Hall effect current have revealed that crystalline grains have good quality and defect states concentrated at grain boundaries for laser crystallized silicon films. The defects can trap free carriers so that they affect carrier transport in polycrystalline films. Reduction of defects by post annealing is important for application of device fabrication. We have developed simple heat treatments with oxygen plasma as well as high-pressure H₂O vapor [14,15] for passivation of silicon grain boundary and surface. 50 nm-thick amorphous silicon films doped with 7.4×10^{17} cm⁻³ phosphorus atoms were crystallized at room temperature in vacuum by laser irradiation at 400 mJ/cm². 1) Samples were treated with 130-Pa-oxygen radio frequency (RF) plasma at 30 W and at 250°C, immediately after crystallization. 2) After crystallization, samples were also heated in high-pressure H₂O vapor with a pressure-proof stainless-steel chamber.

Figure 3 shows the electrical conductivity of silicon films crystallized at 400 mJ/cm² as a function of the reciprocal absolute temperature for different

conditions of treatments of oxygen plasma (a) and H₂O vapor heating (b). As-crystallized silicon films had very low electrical conductivity at room temperature. The electrical conductivity rapidly increased with a high activation energy as the temperature increased. Our recent study using ESR measurements has revealed that rapid formation of crystalline grains results in a high density of dangling bonds about 10^{18} cm⁻³ at their boundaries for laser crystallization. The defects caused by the dangling bonds trap free electrons generated from ionized phosphorus atoms so that grain boundary region has the depletion states with a low electrical conductivity. Marked increase in the electrical conductivity and decreases in the activation energy were observed after the both of oxygen and H₂O treatments. Those treatment made the defects electrically inactive and changed the localized electron states to extended states

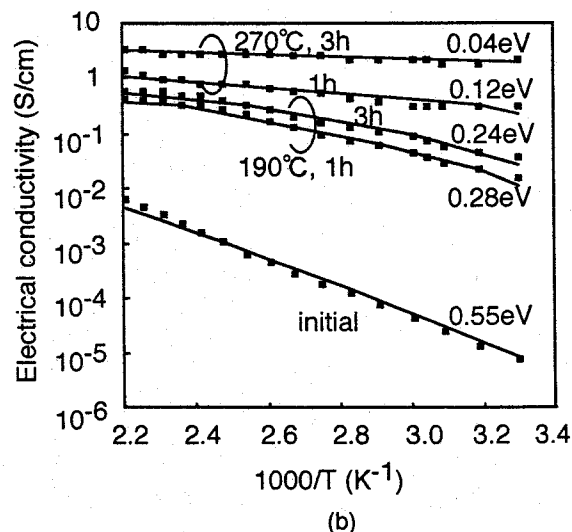
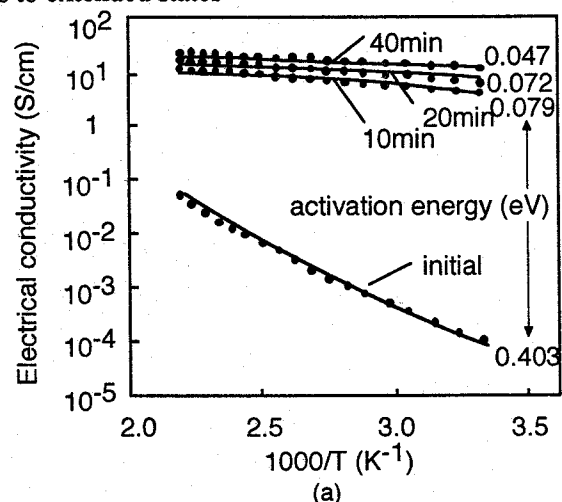


Fig. 3 Temperature dependence of the electrical conductivity for 7.4×10^{17} cm⁻³-phosphorus-doped silicon films 50 nm-thick crystallized at 400 mJ/cm² treated with RF-oxygen plasma at 30 W and as crystallized at 250°C (solid circles) (a) and annealed with 1.3×10^6 Pa-H₂O vapor and as crystallized at room temperature (solid circles) (b). Solid curves are calculated conductivity using our model.

In order to understand the temperature behaviors of the electrical conductivity, we analyzed the electrical conductivity for pulsed laser crystallized polycrystalline silicon films using a two-dimensional numerical analysis program with the finite-element method (FEM) combined with statistical thermodynamical conditions [15,16]. We introduced acceptor type defects at a deep energy level with a Gaussian type density distribution localized at grain boundaries. The charge neutrality is always maintained among the densities of ionized dopant atoms (N_d), negatively charged defect (X_d) and free carriers (n) $\{ N_d = n + X_d \}$ in the entire region including crystalline grains and grain boundaries. The statistical thermodynamical conditions with the Fermi-Dirac statistical distribution function give densities of electron free carriers, ionized donors and the negatively charged defect states, which depends on temperature. Minimizing the electrostatic energy in the entire region with maintaining the charge neutrality conditions gives spatial distribution of the potential energy of the conduction band edge. The spatial distribution of the potential energy of the conduction band edge is governed by the positive space charge effect in crystalline grains around the boundaries as well as the effect of negative charges localized at grain boundaries owing to defects trapping electrons. The effective carrier density in the lateral direction is calculated because the band bending causes a distribution of the free carrier density in the lateral direction and electrical current must traverse grain boundaries. The effective carrier density in the lateral direction is obtained from integration of the reciprocal number of carrier density in crystalline grains. We also introduced scattering effects due to dopant ions, lattice vibration and disordered states at grain boundaries, which reduced the carrier mobility[18]. Defect reduction process was also introduced in the calculation program. H_2O molecules or O atoms incorporate into the silicon films and their density distributes as the complementary error function in the depth direction. The density of the defect states is assumed to be reduced in proportion to the reaction probability and the density of the atoms incorporated in the films. The fitting process between temperature dependences of calculated and experimental conductivities as shown in Fig.3, gives changes in the density of defect states and the potential barrier height at grain boundaries caused by oxygen plasma treatment (a) and high-pressure H_2O vapor annealing (b) as shown in Fig.4. The initial density of defect states was analyzed as 4×10^{17} and $8 \times 10^{17} \text{ cm}^{-3}$ for as crystallized silicon films at 250°C and room temperature, respectively. For as crystallized case at 400 mJ/cm^2 , the potential barrier height was very high, 0.3 eV caused by the density of defect states trapping free electrons. The density of defect state was reduced less than $1 \times 10^{17} \text{ cm}^{-3}$ as the duration of oxygen plasma increased and as the temperature of $1.3 \times 10^6 \text{ Pa-H}_2\text{O}$

vapor annealing for 3 h increased. According to the reduction of the density of defect states, the potential barrier height was reduced to 0.002 eV . The low potential barrier height made electrons go across the barrier at room temperatures so that the effective free carrier density increased. The potential barrier height is essential for carrier transportation. These experimental and analytical results revealed that the two treatments effectively reduced the density of defect states in the laser crystallized silicon films. The defect states were probably oxidized by oxygen plasma or H_2O molecules and became electrically inactive.

We have also revealed that heat treatment with high-pressure H_2O vapor is effective for improvement of SiO_2 properties and SiO_2/Si interfaces[18]. The density of interface trap states is reduced to on the order of $10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ by the treatment at temperature lower than 300°C .

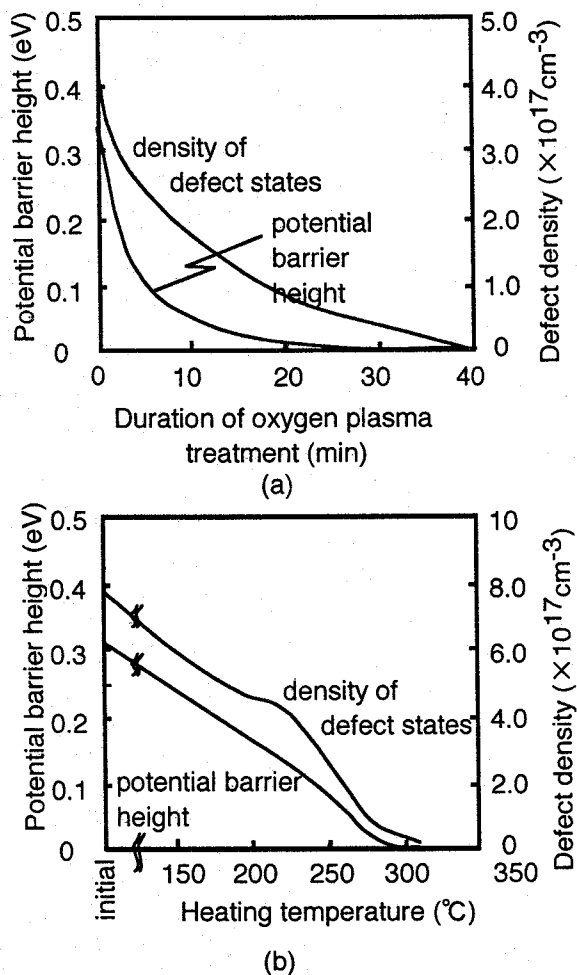


Fig.4 Calculated density of defect states and potential barrier height at grain boundaries as functions of duration of oxygen plasma at 250°C (a) and temperature for heat treatment with and $1.3 \times 10^6 \text{ Pa-H}_2\text{O}$ vapor for 3 h (b).

4. TFT application

Laser crystallization and the heat treatments with oxygen plasma and high-pressure H₂O vapor were applied to fabrication n-channel-top-gate-type poly-Si TFTs [19]. 50-nm thick amorphous silicon films were crystallized in vacuum at laser energy density of 380-440 mJ/cm². Immediately after crystallization, the silicon films were treated with oxygen plasma at 250°C, 130 Pa and 30 W for 40 minutes. Electron cyclotron plasma CVD was used to form 100-nm-thick SiO₂ films at 200 °C. Ion implantation was used to form source and drain regions self-aligned. After TFT fabrication, the TFTs were then heated for 3h at 270°C with 1.3×10⁶ Pa-H₂O vapor. Figure 5 shows transfer characteristics TFTs. Although the TFT fabricated with no oxygen plasma or H₂O vapor heat treatment showed low drain current with a carrier mobility of 87 cm²/Vs. and a high threshold voltage 3.8 V, the TFT fabricated with oxygen plasma showed high drain current with a high carrier mobility of 130 cm²/Vs and a low threshold voltage of 2.8 V. The mobility and threshold voltage were also improved to 105 cm²/Vs and 2.7 V, respectively by high pressure H₂O vapor annealing after TFT fabrication. Both treatment with oxygen plasma after crystallization and high pressure H₂O vapor after TFT fabrication marked improved transfer characteristics as shown in Fig.5. The carrier mobility was 160 cm²/Vs. The threshold voltage decreased to 1.3 V.

We estimated the energy distribution of defect states from the transfer characteristics in the subthreshold region. When the carrier mobility is assumed by the maximum inversion layer mobility obtained at a weak electrical field induced by low gate voltage application, the electrical conductance gives the carrier density and the Fermi level. The gate voltage causes change in the potential in the channel region, which determines the Fermi level and the density of free carrier. It also causes the carrier trapping at defect states. Under the condition of the charge neutrality condition between the gate electrode and at channel region, measurement of change in the electrical conductivity with changing the gate voltage gives energy distribution of the density of defect states, $n_t(E)$ which can trap electron as the following equation,

$$\Delta \left(\int_{0.55}^{1.1} n_t(E) f(E, E_f, T) dE \right) = \frac{C_{ox}}{eD} \Delta V_g - \Delta n$$

$$\Delta E_f = \frac{kT \Delta n}{n} \quad (1)$$

where $f(E, E_f, T)$ is the Fermi-Dirac statistical distribution function as functions of the Fermi energy

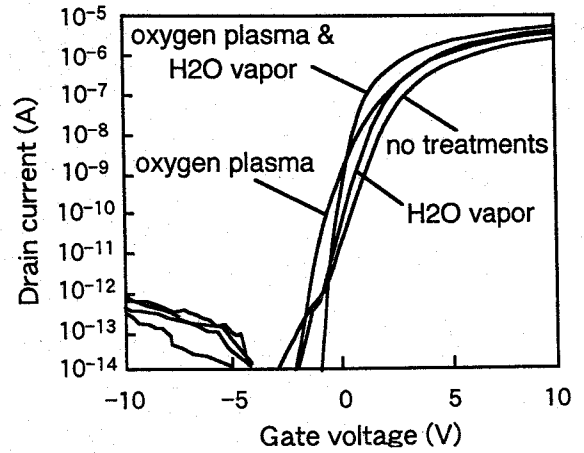


Fig. 5 Transfer characteristics of the TFTs fabricated with no oxygen plasma or no high pressure H₂O vapor heating, with treatment with oxygen plasma, with H₂O vapor annealing and with oxygen plasma followed by high pressure H₂O vapor annealing. Oxygen plasma treatment was carried out at 250°C for 40 min. at 30W at oxygen gas pressure 130 Pa. The High pressure H₂O vapor annealing was at 270°C at 1.3×10⁶Pa for 3h. The drain voltage was 0.1V. The ratio of channel width to channel length was 1.

(E_f) and the absolute temperature (T), C_{ox} is the gate capacitance per unit area, e is the elemental charge, D is the silicon film thickness, n is the density of free carrier and k is the Boltzmann constant.

Figure 6 shows the density of the gap states as a function of energy in the band gap for TFTs explained above. High densities of broad tail states and sharp peak of deep states with a width of about 0.1 eV around the mid gap were estimated for TFT fabricated with no treatment for defect reduction. For TFT with oxygen treatment after crystallization, marked reduction in defect density at the deep energy level was observed, although the density of defect states near the conduction band region was still high. Localized dangling bonds at grain boundaries were probably oxidized by oxygen plasma treatment and made electrically inactive. Reduction in the density of state at the deep energy level resulted in marked increase in the drain current with application of a small gate voltage. However high residual density of gap states at shallow energy level did not allow a low enough threshold voltage. On the other hand, reduction in the defect density was observed in the entire region in the band gap for the TFT annealed

in high pressure H_2O vapor after fabrication. Sharp peak of density of states at the deep level remained after H_2O vapor. Reduction of dangling bonds by H_2O vapor annealing were not effective compared with oxygen plasma in the present experimental conditions. The reduction of the density of states in the entire energy range suggests that the H_2O vapor annealing reduces the density of gap states induced from disordered bonding network at SiO_2/Si and grain boundaries. Marked reduction in the density of gap states to $\sim 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ was achieved by combination of oxygen plasma with H_2O vapor annealing, as shown in Fig.6. The density of defect states at shallow levels especially reduced by High pressure H_2O vapor annealing after oxygen plasma treatment. The low density of defect states resulted in high performance of TFTs especially with a low threshold voltage of 1.3 V. These results show that the present heat treatments are useful for defect reduction and surface passivation to device fabrication processing.

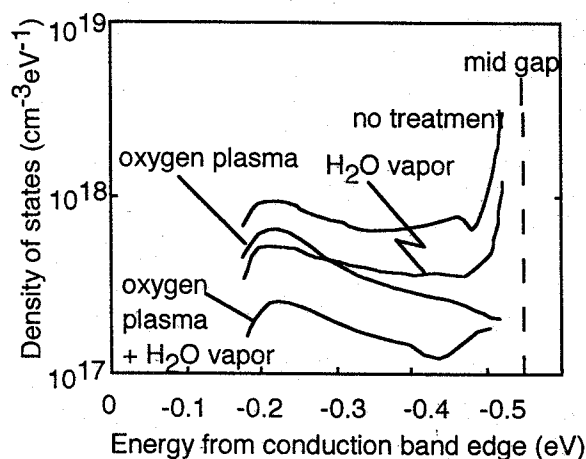


Fig.6 Density of gap states estimated from subthreshold characteristics using eq.(1) as a function of energy

5. Large grain growth using electrical current induced joule heating

We report a crystallization method with pulsed electrical current induced heating of silicon films in order to fabricate large crystalline grains [20,21]. The voltages were applied to 60-nm-thick silicon films doped with phosphorus atoms at $7.4 \times 10^{17} \text{ cm}^{-3}$ formed on glass substrates via a simple electrical circuit with a capacitance connected to silicon films in parallel as shown in inset in Fig.7. Simultaneous with voltage application, samples were irradiated by a 30-ns-pulsed XeCl excimer laser to melt the silicon films partially. Although silicon films have high resistivity in the solid phase at room temperature because of a low carrier

density, the resistance of silicon markedly decreases when it is melted, because liquid silicon has a metallic phase. Laser-induced melting during voltage application therefore leads to a high joule heating per unit area induced by the electrical current, $I^2 R_S / S$, where S is the area (width x length) of silicon films.

Figure 7 shows changes in the electrical current flowing in the silicon films obtained experimentally with a capacitance of $2.0 \mu\text{F}$ as a function of time. High electrical current was observed by laser irradiation at 400 mJ/cm^2 due to rapid melting of silicon films. The electrical current was still observed after the termination of laser pulse due to the electrical-current-induced joule heating. Figure 7 also shows the calculated change in the electrical current flowing in the silicon films with a time constant under the assumption that the silicon film was completely melted and had a constant and minimum resistance. Both experimental and calculated electrical currents decreased for $42 \mu\text{s}$ keeping the same current. This means that the resistance of silicon films did not change because the current-induced joule heating kept the silicon at the melted state. However, rapid decrease in the electrical current due to increase of the resistance of silicon associated with solidification was observed from the point indicated by arrows in Fig.7. The solidification duration was $28 \mu\text{s}$ for the capacitance of $2 \mu\text{F}$. The present current-induced joule heating makes it possible to control the melt duration and the solidification duration, which are important parameters in the crystallization of silicon films with a simple electrical circuit.

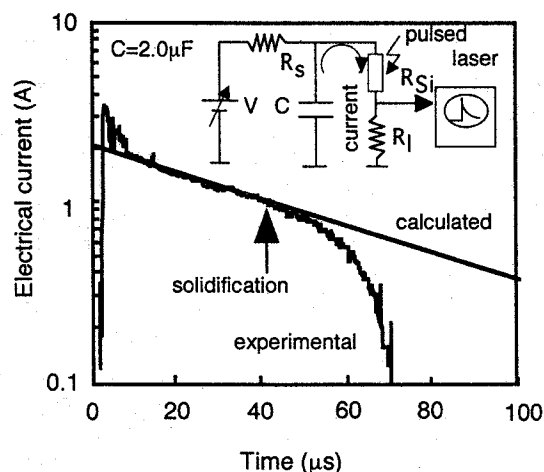
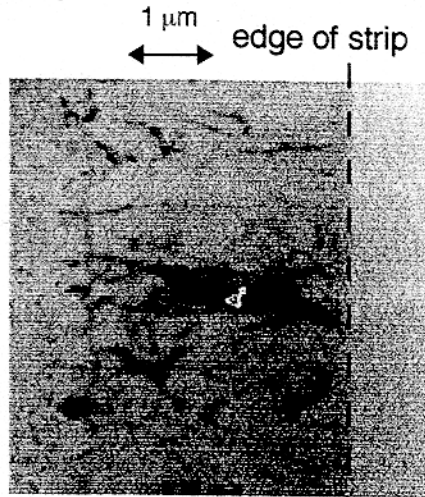


Fig.7. Changes in the electrical current flowing in 60-nm thick silicon stripes. The samples were heated by laser irradiation at 400 mJ/cm^2 during application of a voltage at 130 V. Equivalent circuit is shown in the inset. Series resistance R_S and load resistance R_L were

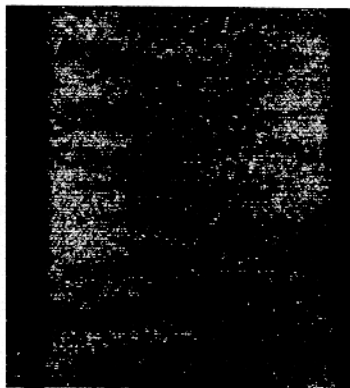
1K Ω and 5 Ω .

Figure 8(a) shows a photograph of the bright-field image of transmission electron microscope at edge region of silicon stripes crystallized at 0.22 μ F. The preferential crystalline orientation of (110) was determined. The distribution of preferential orientation was pulse or minus one degree among the crystalline grains. Figure 8(b) shows a photograph of the distribution of crystalline grains treated slightly by Secco etching in the case of crystallization with at a capacitance of 1.0 μ F. Formation of crystalline grains about 15 μ m long were observed. The large grain growth at the edge region indicates that crystallization initiated at the edge of the silicon stripes and proceeded inside because there were temperature gradient at the edge region due to high heat dissipation from the edges. These results indicate the possibility of crystalline grain growth in the lateral direction using the present heating method and with a certain method for formation of temperature gradient.



(a)

10 μ m



(b)

Fig. 8. Photographs of the bright field image at the edge region of silicon stripes crystallized by the electrical current induced joule heating method with a

capacitance of 0.22 μ F (a) and of Secco etched films crystallized at at 1.0 μ F (b).

Figure 9 shows the electrical conductivity as a function of reciprocal absolute temperature for 7.4×10^{17} cm⁻³ phosphorus-doped silicon films crystallized by the electrical current induced joule heating at capacitance of 0.11 and 0.22 μ F and at zero capacitance, as well as for simple laser crystallization at 400 mJ/cm². For simple laser crystallization, the electrical conductivity was very low at room temperature due to the high defect density. On the other hand, high electrical conductivity was observed for the electrical-current-induced joule heating cases and the activation energy decreased, as shown in Fig. 9. Analyses of changes in the electrical conductivity using a statistical thermodynamical analysis program previously discussed suggested that the density of defect states was lower than 1.3×10^{12} cm⁻², which was much lower than that of 3.8×10^{12} cm⁻² for silicon films formed by laser crystallization. These results suggest that the present current induced joule heating has the possibility of formation of high quality polycrystalline films.

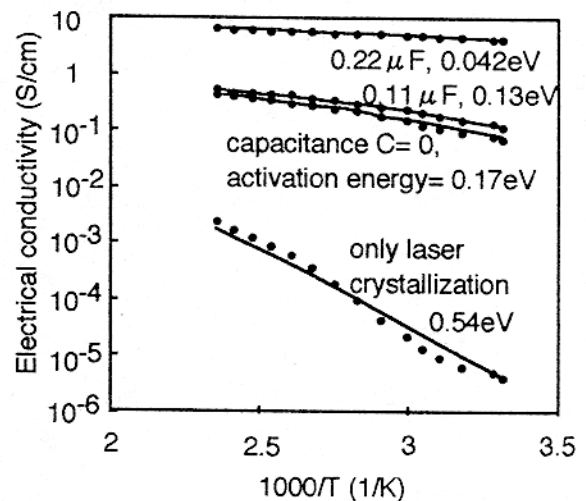


Fig. 9 Electrical conductivity measured (dotted curves) and calculated (solid curves) as a function of reciprocal absolute temperature for 7.4×10^{17} cm⁻³ phosphorus-doped silicon films crystallized at 0.11, 0.22 μ F and zero capacitance as well as for simple laser crystallization at 400mJ/cm²..

6. Summary

Fundamental properties of pulsed laser silicon films were discussed. The silicon films were melted by

rapid heating of pulsed laser irradiation and then solidified to crystallize state. Crystallization initiated from the bottom region in the films. Analyses of free carrier optical absorption and Hall effect current measurements of doped polycrystalline films revealed that the crystalline grains had good electrical properties although the crystalline grain size was as small as at ~ 10 nm and that there was substantial disordered states between crystalline grain, which reduced the carrier mobility of electrical currents traversing grain boundaries. The carrier mobility obtained by the Hall effect measurements markedly increased to $28 \text{ cm}^2/\text{Vs}$ as the laser energy density increased to $360 \text{ mJ}/\text{cm}^2$ because of improvement of grain boundary properties for $2.5 \times 10^{20} \text{ cm}^{-3}$ doped films.

The heat treatment methods were developed for reduction of the density of defect states. Oxygen plasma annealing at 250°C and high-pressure $1.3 \times 10^6 \text{ Pa}$ - H_2O vapor annealing at $\sim 300^\circ\text{C}$ were used to reduce the density of defect. The treatments made defect states electrically inactive so that most of the electron produced from dopant atoms became conductive. Improvements of electrical properties according to reduction of defect states were analyzed using a two-dimensional numerical analysis program with statistical thermodynamical conditions. Minimizing the electrostatic energy in the entire region with maintaining the charge neutrality conditions gave spatial distribution of the potential energy of the conduction band edge. The defect density was reduced from $\sim 10^{18} \text{ cm}^{-3}$ to less than 10^{17} cm^{-3} and the potential barrier heights at grain boundaries decreased to from 0.3 eV 0.002 eV . Those heat treatment were applied to fabricate the polycrystalline silicon thin film transistors fabricated in laser crystallized silicon films. The density of gap states was markedly reduced in entire region of band gap by oxygen plasma treatment after crystallization and high pressure H_2O vapor annealing after fabrication process. These treatments resulted in a high carrier mobility at $160 \text{ cm}^2/\text{Vs}$ and a low threshold voltage of 1.3 V .

We demonstrated electrical-current-induced joule heating for crystallization of silicon films. The joule heating from electrical energy accumulated at the capacitance caused the crystalline grain formation with a size of $15 \mu\text{m}$. Preferential crystalline orientation normal direction to substrate was (110). The density of the defect state at grain boundary plane was estimated about $1.3 \times 10^{12} \text{ cm}^{-2}$.

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Crystalline thin-film silicon solar cells from layer-transfer processes: a review

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Abstract: Layer transfer processes provide a new and largely unexplored route for the fabrication of highly efficient monocrystalline thin-film Si solar cells. Monocrystalline Si wafers serve as a substrate for epitaxial growth. A special surface conditioning of the substrate permits the transfer of a thin epitaxial film to an arbitrary carrier substrate. The growth substrate is then re-used to fabricate further cells. The possibility to use different materials for growing the thin film and for carrying the devices broadens the design flexibility and opens a new path for cost reduction. We describe and discuss the various layer transfer processes that are currently being developed for Si. A particularly important point to work on in the future is the demonstration of the frequent re-use of the substrate and the development of a large-area and low-cost epitaxy technique.

1 Introduction

Crystalline Si photovoltaics benefits from more than half a century of experience in Si microelectronics. The photovoltaic material Si is abundant in the earth's crust and is environmentally benign. The main obstacle for a wider spread of crystalline silicon photovoltaics is the high cost of crystalline Si wafers that have a typical thickness of 300 μm and account for more than 50% of the module costs. The reduction of Si consumption is the driving force for the world-wide increasing interest in the development of thin-film modules. Crystalline Si solar cells are termed "thin" if the effective thickness is less than 50 μm ; that is approximately a tenth of the wafer thickness. The effective thickness W_{eff} is the ratio of cell volume over macroscopic cell area.

A cell efficiency of 15% is necessary for thin-film cells to compete with wafer cells that are a "moving target" for all thin-film technologies. For crystalline Si a large variety of deposition techniques, substrates, and cell designs are currently under investigation [BER1999]. Most of these developments are in the laboratory phase resulting in solar cells of a few cm^2 in area. This review paper gives a short introduction to Si thin-film cells, derives criteria for efficiencies above 15%, and then focuses on layer transfer processes (LTP). The LTP are a particularly promising approach because they circumvent the key difficulties of the more conventional approaches. We describe the previous work in the young and rapidly developing field of LTP and also discuss the future challenges.

2 Crystalline thin-film cells

Crystalline Si has a small optical absorption coefficient in the near infrared spectral region. Therefore thin-film cells from crystalline Si have to use light trapping schemes to enhance the optical absorption. Lambertian light trapping [GOE1981] is frequently used as a benchmark for the good optical performance. Experiments demonstrated that a close to Lambertian light scattering behavior is experimentally feasible [POR1998]. With Lambertian light trapping a 1- μm -thick cell absorbs approximately as many solar photons as a 50- μm -thick cell without light trapping. A path length enhancement by about a factor of 50 is possible [YAB1982].

Figure 1 shows thin-film solar cell efficiencies that we calculate for ideal Lambertian light trapping (solid lines) and without light trapping (broken lines). The highest efficiencies are achieved if the cell is limited by intrinsic recombination mechanisms, that is radiative recombination and Auger recombination. Efficiencies of 26% are theoretically feasible with a 1- μm -thick cell while only 9% are feasible without light trapping. Defect recombination such as surface recombination is in practice important. Assuming a surface recombination velocity of 100 cm/s and a p-type base doping of 10^{17} cm^{-3} limits the efficiency to 18% for a 1- μm -thick cell with and to 6% without light trapping. The efficiency is 12% with and 4% without light trapping in fine-grained polycrystalline material with a grain boundary recombination velocity of 10^4 cm/s and a grain size g equal to 100 nm. In all cases light trapping increases the efficiency by a factor of 3 for a 1- μm -thick cell. Innovative cell designs such as the parallel multijunction concept [GRE1994] or the Encapsulated-V design [BRE1995c] de-couple the optical and the electrical thickness and serve to approximate the infinite mobility assumption underlying the efficiency calculations of Figure 1. Cell efficiencies well above 15% are possible at thickness values of only a few microns provided (i) efficient light trapping is used, (ii) surfaces are passivated to a surface recombination velocity level of around 100 cm/s , and (iii) grain boundary recombination is negligible.

We classify the experimental approaches to fabricate highly efficient thin-film cells into four classes [BRE1999]:

Wafer cells (WC) that reach encouraging efficiencies above 19% [BRE1995d, GRE1995, GLU1997]. However, the processes consume a full Si-wafer and use photolithography. These types of cells are not cost effective.

Cells on high temperature substrates (HTS) are typically fabricated at temperatures above 1000°C. Efficiencies up to 11% were reached with a polycrystalline Si layer of 15 μm in thickness and without light trapping [AUE1997, LUE1997]. The grain size is in the 100 μm range. Hence grain boundaries are of minor importance for the electronic transport. Introduction of light trapping, e.g. by light scattering due to sintered porous inter-layers [MUE2000] or by using highly reflective ceramic substrates [FOR1999], is important to further enhance the efficiency. However, the major challenge for the HTS approach to

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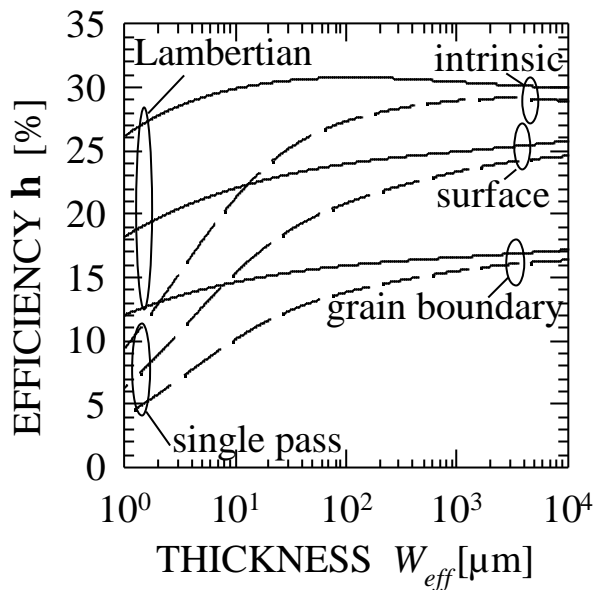


Figure 1: Efficiency estimates in the infinite mobility limit for cells with Lambertian light trapping (solid lines) and cells without light trapping (broken lines). Intrinsic recombination, surface recombination ($S = 100$ cm/s) at base doping 10^{17} cm $^{-3}$, and grain boundary recombination ($S = 10^4$ cm/s, $W_{eff}/G = 10$) are considered. One sun AM1.5G illumination [HUL1985] is assumed.

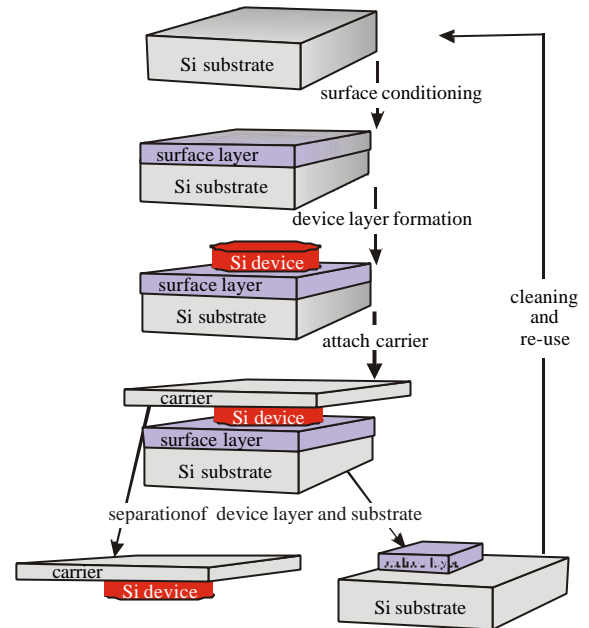


Figure 2: The layer transfer process starts with a Si substrate that receives a surface conditioning. After film growth, a carrier is attached to the device layer to enhance the mechanical strength of the device layer. The surface conditioning permits a detachment of the device layer. The Si substrate re-used for further layer fabrication.

crystalline thin-film cells is the development of a high-temperature resistant *and* low-cost substrate that is sufficiently inert, pure, and flat not to interact with molten Si during the zone melt recrystallization (ZMR). Such a substrate is currently not described in the literature.

Cells on low temperature substrates (LTS) are deposited at temperatures ranging from 200°C to 550°C. Low cost substrates such as glass, metal, or plastics are being used. Efficiencies of 10.1% have been reported for films of 2 μm in thickness with light trapping [YAM1999]. The small deposition temperature reduces the surface mobility of the reactive species and thus causes a more defective material with small grains in the 100 nm range. Grain boundary recombination is likely to play an important role for the transport [BRA2000]. The low surface mobility and the large hydrogen dilution that causes Si etching bring along a small growth rate in the range of a few Angstrom/s. A significant enhancement of the growth rate is necessary to make this approach economically viable.

Cells from layer transfer processes (LTP) use the process that is schematically sketched in Figure 2. A special surface conditioning of the growth substrate permits the transfer of the device layer from a re-usable growth substrate to a low-cost device carrier. Using a monocrystalline Si wafer as the growth substrate permits to fabricate monocrystalline cells by homoepitaxy that fully avoid grain boundary recombination. Since Si withstands high temperatures, high growth rates are easily feasible. The high cost of the Si substrate is not a problem if the substrate wafer is re-used frequently. The carrier does not have to withstand high temperatures and is therefore low cost. In contrast to the HTS and LTS approaches both surfaces of the device are freely accessible during the process. Hence both surface may be passivated with standard technologies developed for wafer cells [LAU1996]. Textured thin-films for light trapping are readily realized by growing the device layer on textured substrates [BRE1997]. Hence the above mentioned conditions (i), (ii) and (iii) for high conversion efficiencies can be met while specific disadvantages of the LTS and HTS approach are circumvented. In this paper we review the previous work on layer transfer processes.

3 Layer transfer concepts for Si

Layer transfer for solar cell fabrication was invented by McClelland et al. to reduce the fabrication costs of GaAs cells, a particularly costly PV material [MCC1980]. With the CLEFT (cleavage of lateral epitaxial films for transfer) process McClelland et al. grew single crystalline GaAs films by vapor phase epitaxy on re-usable GaAs substrates. A carbonized photoresist mask with stripe openings is deposited onto the GaAs wafer. The openings function as a seed and lateral overgrowth produces a continuous film that is a single crystal. The film surface is then bonded to a glass and the film is cleaved from the substrate. The material quality of the film was found to be comparable to films grown on substrates without a mask. A 17% efficient GaAs cell with a thickness of 10 μm [BOZ1981] and the four-fold use of the substrate was demonstrated [MCC1980]. This original work already suggested to apply layer transfer processes also to other semiconductor materials. Landis proposed to grow an epitaxial Si film on a textured Si wafer covered with a lattice matched salt [LAN1990]; however this process has never been verified experimentally. More than a decade after the introduction of the CLEFT process a number

of Si layer transfer processes are now being developed. We describe these layer transfer processes in this section in historical order.

3.1 Via hole etching for the separation of thin films (VEST)

Deguchi et al. fabricated a Si solar cell by layer transfer using the VEST (via hole etching for the separation of thin films) process that is currently investigated at Mitsubishi [DEG1994, ARI1994]. The process starts with a monocrystalline Si wafer that is oxidized (surface conditioning). The oxidized wafer serves as the substrate for the fabrication of a large-grained polycrystalline Si film by ZMR. The re-crystallized layer is then thickened by chemical vapor deposition (CVD) and randomly textured by KOH etching. Wet chemical etching of the SiO₂ inter-layer through via-holes in the epitaxial layer detaches the device layer.

The via-holes are used to fabricate an emitter-wrap-through structure [GEE1993] that reduces the grid shadowing, simplifies the series interconnection [MOR1999], and enhances carrier collection [PLI1998]. Multicrystalline cells of about 80 μm in thickness achieve efficiencies of 16% on areas of 100 cm² [ISH1998] and 13% on 924 cm² [MOR1999]. Thin-film cells with thickness below 50 μm were not reported.

3.2 Epitaxial layer transfer (ELTRAN)

The successful transfer of a *monocrystalline* Si film was demonstrated by Yonehara et al. using the ELTRAN (epitaxial layer transfer) process developed at Canon [YON1994]. The top 10 μm of a planar monocrystalline Si wafer are transformed into porous Si by anodic etching [ALO1997] in aqueous hydrofluoric acid (surface conditioning). The typical pore diameter is around 50 nm. The porous Si is then oxidized in order to stabilize it against re-organization during high temperature processing. A HF-dip removes the oxide at the outer surface and annealing the porous Si in hydrogen at temperatures around 1000°C closes the pores at the sample surface [SAT1995] which is an ideal starting condition for the CVD epitaxy process. The epitaxial layer is then bonded to an oxidized carrier wafer and the substrate wafer is sacrificed by grinding it down to the porous Si layer [YON1994]. The inner surface of the stabilized porous Si remains large and thus porous Si is etched with a selectivity of 10⁵ against bulk Si [SAK1995]. The high selectivity results in a planar surface of the transferred epitaxial Si layer that is further smoothed by annealing in hydrogen.

Silicon on insulator (SOI) wafers fabricated by ELTRAN are now available commercially [YON2000a]. No solar cell results applying the ELTRAN process have been reported.

3.3 Smart Cut (SC) process

The Smart Cut (SC) process introduced by Bruel [BRU1995, BRU1996] demonstrated the re-use of the Si substrate after layer transfer. The substrate is again a monocrystalline Si wafer. However, for surface conditioning hydrogen ions are implanted into the Si wafer to a well controlled depth. The Si wafer is then bonded to an oxidized carrier wafer. Heating the whole system to temperatures around 500 °C causes the implanted hydrogen to expand and to split off the thin Si layer.

The SC process aims at the SOI market and has not yet been applied to solar cell fabrication. The thickness of the transferred layer is defined by the penetration depth of the H⁺ ions which is typically less than 1 μm . This fact and the necessity of ion implantation limits the applicability of the SC process to PV.

3.4 Sacrificial porous Si (SPS) process

Tayanaka et al. introduced a layer transfer process [TAY1996] that we name *sacrificial porous Si* (SPS) process in this paper. The SPS process is now being developed at Sony [TAY1996, TAY1998] and at the University of Stuttgart [BER1999a]. Similar to ELTRAN, CVD on a porous Si is used. However, a porous multilayer system with a low surface porosity and a high porosity in the depth is used to permit high quality epitaxial growth and subsequent detachment of the epitaxial layer. Since no stabilization of the porous Si by thermal oxidation is used, the surface and the volume of the porous multilayer re-organizes during annealing and epitaxy: the surface closes (as for ELTRAN) and voids form in the volume of the low-porosity layer. The high porosity layer transforms into weak Si bridges. Our Monte Carlo simulations demonstrated that the only driving force necessary to explain these re-organization is a reduction of surface energy [MUE2000a]. The cell is then attached to a flexible plastic film and detached by applying tensile mechanical stress that breaks the weak Si bridges.

The sintered low-porosity layer forms the back of the solar cell and the voids introduce some degree of light trapping. Outstanding solar cell results were recently reported with a 12 μm -thick monocrystalline Si cell achieving an efficiency of 12.5% [TAY1998] and a 24 μm -thick cell achieving an efficiency of 14.0% [RIN2000]. The latter value achieved at the University of Stuttgart is currently the highest efficiency of a truly thin-film cell reported until today. A minority carrier lifetime corresponding to a diffusion length of 500 μm was reported for the SPS process [TAY1999].

3.5 Porous Si (PSI) process

The *porous silicon* (PSI) process was introduced by Brendel [BRE1997] and is being developed at the Bavarian Center of Applied Energy Research (ZAE Bayern). The PSI process was the first demonstration of the fabrication of a textured monocrystalline Si film using porous Si for layer transfer. In contrast to the SPS process we start from a textured wafer. A Si film grows on a porous double layer by ion assisted deposition [OEL1994] at temperatures around 700°C [BRE1997]. Similar to the ELTRAN process the porous Si is stabilized by oxidation to maintain the microstructure. A glass is then attached to the front surface with a transparent glue and mechanical stress splits the cell from the substrate at the position of the buried high-

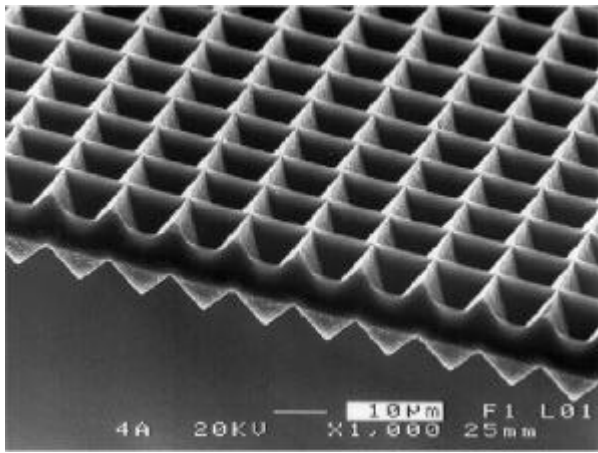


Figure 3: Perspective SEM-top view of a free standing Si waffle produced by the PSI process using ion-assisted deposition on substrates textured with regular pyramids.

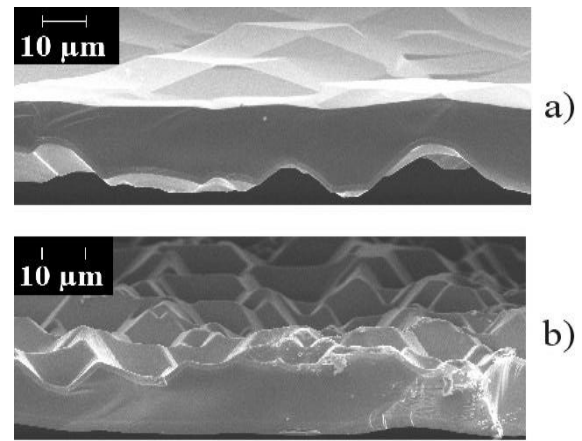


Figure 4: SEM micrographs of detached silicon film fabricated by the PSI process: a) a 15- μm -thick CVD-film deposited on a randomly textured substrate, b) same film from the substrate side showing random inverted pyramids.

porosity layer. Residual porous Si is removed by an air jet. Figure 3 shows the scanning electron microscope image of a free standing Si waffle with conformal front and back surface. Extensive modeling of the waffle-shaped cell demonstrated an efficiency potential above 17% for film thickness values $W_{\text{eff}} < 5 \mu\text{m}$ [BRE1999b]. We also used CVD deposition at 1100°C on randomly textured growth-substrates with a porous multi-layer structure [KUC2000]. Figure 4a shows a SEM micrograph of a 15-micron-thick monocrystalline silicon film. The CVD deposition smoothes the pyramid texture and the top-side is almost planar showing facets with a small inclination of 8° . Figure 4b shows the film as viewed obliquely onto the substrate side. This surface is textured with *random inverted* pyramids. This is a novel type of surface texture that has a light trapping performance similar to that of the regular waffle shown in Figure 3. The material quality of our CVD layers is currently superior to our IAD material quality [KUC2000]. This is primarily due to the higher deposition temperature.

Cell efficiencies using a waffle-shaped Si film have not yet been published. The minority carrier diffusion length is $3 \mu\text{m}$ in a $7 \mu\text{m}$ -thick planar IAD film while it exceeds the film thickness for the CVD film.

3.6 Epilift (EL) process

The Epilift (EL) process was introduced by Weber et al. [WEB1997, WEB1998] and is developed at the Univ. Canberra. The EL is a layer transfer technique that starts with a (100)-oriented monocrystalline Si wafer as the growth substrate. A mesh-patterned silicon oxide layer is processed onto the surface of the wafer by photolithography. The lines of the mesh run in (110) direction. An epitaxial layer is then grown by liquid phase epitaxy (LPE) exposing (111)-oriented facets. The cross section of the Si mesh growing in the seed lines is diamond-shaped. At the end of the growth process the silicon containing metal solution escapes through the mesh openings. Typical film thickness values are 50 to $100 \mu\text{m}$. Effective thickness values of only a few microns are claimed to be also possible with the EL process [WEB1999]. The Si mesh is detached by wet chemical or electrochemical etching [WEB1999]. The EL shares the idea of epitaxial lateral overgrowth through line-shaped seeds defined by a patterned cover with the CLEFT process. However the mesh is a continuous seed and therefore no merging of separate crystals occurs in the EL process.

Transient photoconductance decay measurements revealed minority carrier diffusion lengths of $100 \mu\text{m}$ [CAT1998]. Efficient light trapping in the Si meshes was demonstrated on the basis of theoretical light trapping studies. However, no cell efficiencies have yet been reported. Using substrates of various orientations a wide variety of cell layer shapes may be fabricated [WEB1998].

3.7 Quasi monocrystalline Si (QMS) process

The quasi-monocrystalline Si process (QMS) was introduced by Rinke et al. [RIN1999] and is under development at the University of Stuttgart. The QMS process is identical to the SPS process but the sintered porous Si layer is not used as a seed for epitaxy but as the device layer. The great advantage of this approach is that no epitaxy is required. The voids in the sintered porous Si layer introduce light trapping in a device with planar surfaces. Surface texturing of the substrate as in the PSI process is avoided. A short circuit current density of $11.1 \text{ mA}/\text{cm}^2$ was measured for a $4 \mu\text{m}$ -thick sintered porous Si layer prior to detachment from a p-type wafer of specific resistance of $0.05 \Omega\text{cm}$ [BER2000]. Cell efficiencies were not reported. The fabrication of 30 sintered porous Si films from a single Si wafer was demonstrated.

3.8 Solar cells by liquid phase epitaxy over porous Si (SCLIPS) process

A modified version of the ELTRAN process was recently applied to Si solar cells for the first time [IWA1999]. This process is named SCLIPS (solar cells by liquid phase epitaxy over porous Si) [YON2000]. The epitaxial layer grows by liquid

phase epitaxy using a reactor that rotates the substrates to enhance convection. Growth rates as high as 1 $\mu\text{m}/\text{min}$ are reported. The novel SCLIPS-version of the ELTRAN process re-uses the Si substrate by using a porous multi-layer system similar to the SPS and the PSI process. A water jet splits the device layer from the growth substrate [SAK1999, YON2000].

An average minority carrier lifetimes corresponding to a diffusion length of 160 μm was reported [YON2000] and an efficiency of 9.5% of a small (0.2 cm^2) cell was achieved from a transferred cell with a thickness $W_{\text{eff}} > 10 \mu\text{m}$.

4 Discussion

4.1 Re-usability of growth substrate

The layer transfer concept will only become economically viable for PV applications if the frequent re-use of the substrate is possible. The original version of the ELTRAN process consumes the substrate wafer and is therefore too costly for thin-film photovoltaics. The re-use was experimentally verified for a modified ELTRAN process and the Smart Cut process that both aim at SOI-products. However, for none of the solar cell processes discussed above the multiple re-use of the growth wafer was demonstrated by multiple working solar cells. This crucial point has to be clarified in the near future. The re-use of the substrate becomes easier if the process stresses the growth wafer as little as possible. Hence low temperature processing and in particular low spatial temperature gradients are beneficial. The PSI process using IAD deposition around 700°C stresses the substrate less intense than the VEST process where a small zone of molten Si is pulled across the oxidized Si substrate. I have no doubts that a ten-fold re-use of the substrate is possible with IAD and CVD-deposition.

4.2 Film growth

Chemical vapor deposition at temperatures above 1050°C is the dominating deposition technique in the previous work on layer transfer processes for good reasons. The cost efficiency of a thin-film approach is high, if the device efficiency is high, if little material is consumed (that means a small film thickness W_{eff}), and if the deposition rate is high to keep the residence time in the epitaxial reactor small. Since high deposition temperatures tend to yield better material quality *and* higher deposition rates the use of high temperatures is advantageous for low-cost PV. Hence CVD has an advantage over LPE and IAD. The CVD technique from SiHCl_3 has the additional advantage that CVD process is one step of the Siemens process for the fabrication of any electronic grade Si material. Hence using CVD from SiHCl_3 saves at least one melting and crystallization step when compared to wafer Si. To bring the residence time in the epitaxy reactor into the range of a few minutes the film thickness should be kept in the micron range. The texturing of monocrystalline micron-thick films with random pyramids by KOH etching is probably impossible because the etch depth is not well controlled unless photolithography is used. Deposition on textured substrates with the PSI process permits the fabrication of micron and sub-micron thin cells without using photolithography. With deposition times in the minute range the set up time of the epitaxial reactor becomes important. In-line atmospheric pressure CVD machines similar to the one developed by Faller et al. [FAL1999] are to be preferred over batch-type high-vacuum machines such as IAD. The SCLIPS and the EL processes use LPE which should allow processing of large batches. The QMS process avoids epitaxy and could therefore be cost effective if efficient cells can be fabricated despite the large inner void surface that causes inner surface recombination.

4.3 Surface conditioning

The dominating surface conditioning technique is the formation of porous Si (ELTRAN, SPS, PSI, QMS, SCLIPS). Using porous Si for growth and separation yields closed monocrystalline films in contrast to the VEST process and the EL process. The VEST process has the disadvantage to yield polycrystalline films. A ZMR process is not necessary if porous Si is used for epitaxy and separation. At the present status of the development of the PSI process at ZAE Bayern we find the technological window for a porous Si layer system that permits high quality epitaxy *and* detachment to be rather small. Hence, the application of the stress for separation using a well controlled water jet in the SCLIPS process is certainly of advantage for a high yield. We consider the SC process to be not of relevance for PV because ion implantation is more expensive than porous Si formation and because a thickening of the monocrystalline Si film has to be done either at temperatures below 400°C or after the transfer to a low-cost substrate [BRU1996]. Both possibilities do not permit the use of high temperature and high rate epitaxy.

4.4 Light trapping

High-level light trapping is required to realize efficiencies above 15% in cells that are only a few microns thick. An optical absorption in $W_{\text{eff}} = 10 \mu\text{m}$ thick films that corresponds to a maximum short circuit current density around 36 mA/cm^2 was shown for waffles from the PSI process fabricated by IAD [BRE1997] and CVD [KUC2000], and for Si meshes from the EL process [CAT2000]. The level of light trapping that is achieved by the voids in the sintered porous Si at the back of cells from the SPS process is not yet clear. Surface texturing with photolithographically defined inverted pyramids was shown to enhance light trapping in cells from the SPS process [RIN2000]. Random texturing of planar films is limited to layer thickness values above 30 μm since the etch depth is not well controlled. Using the PSI process micron-thin, textured films are fabricated that realize a path length enhancement factor of around 40 [BRE1999b]. A cell with grids on both surfaces and a detached back reflector behind the cell was found to be an important optical feature that minimizes optical losses in the back

reflector [BRE1999b]. A light trapping scheme using diffraction gratings was suggested for the SPS cells and was calculated to enhance the average path length moderately by a factor of 3 [MIZ1999].

4.5 Surface passivation

A surface recombination velocity around 100 cm/s is feasible for monocrystalline Si with a doping concentration ranging from 10^{16} to 10^{17} cm⁻³ [LAU1996]. In contrast, the passivation level of a thick back surface field with a high-low junction is around 1000 cm/s [BRE1995b]. The surface recombination losses in cells with no back surface field and both surfaces nitride passivated will therefore be smaller than in cells from the SPS process with a metalized and void-containing highly doped back surface field. Removing the void region by etching and passivating should further improve the cell voltage.

4.6 Cell process

The encouraging solar cell efficiencies of 12.5% [TAY1998] and 14% [RIN2000] that were achieved with the SPS process demonstrate the potential of the LTP approach. Both results are achieved with complex high efficiency processes that include diffusion, oxidation, and photolithography. Hence, it is of importance for the LTP approach to develop simpler cell process. One step towards simplification is to grow the emitter [FEL2000] which is faster than thermal diffusion of the emitter. With the exception of the VEST process all previous cells use vacuum evaporation for contact formation. Low-cost fabrication sequences will probably have to use screen printing. The mechanical stress applied to VEST cells during the screen printing process requires a minimum thickness of 80µm for sufficient yield [PLI1998]. Hence the glue used to attach the transferred films to the carrier should be sufficiently hard to permit screen printing. Epitaxy on porous Si yields closed films while the EL and the VEST process have openings in the film. A possible disadvantage of these openings is the necessity of unconventional cell processing.

4.7 Series connection

In addition to thickness reduction, the integrated series connection of solar cells to modules bears a further possibility for cost reduction relative to modules from wired wafer cells. Work on an integrated series connection was reported for the PSI process [BRE1999a] and the SPS process [MAT2000]. The concept for the integrated series connection using the PSI process is shadow-epitaxy (Shadex) through a mask as sketched in Figure 5. Wires spanned in front of the sample avoid epitaxy underneath the mask and thereby define the position of trenches. Moving the sample relative to the mask we demonstrated the in-situ fabrication of a waffle-shaped mini-module containing 6 cells [BRE1999a]. Thin-monocrystalline modules were also fabricated using the SPS process [MAT2000]. Here the individual cells are isolated by oxidized porous Si. In addition to porous Si formation wet chemical etchings, oxidations, and laser ablations are necessary to fabricate the integrated SPS module.

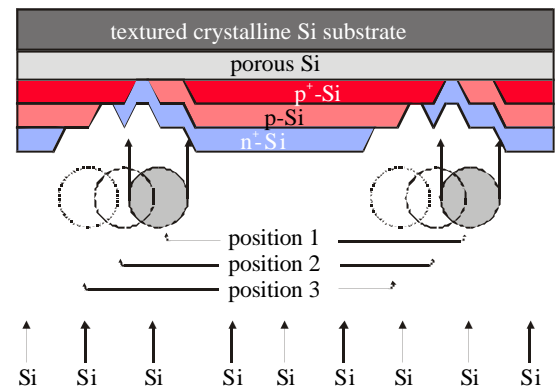


Figure 5: Shadow-epitaxy by ion-assisted deposition fabricates an integrated series connection during film deposition. The pyramidal texture of the substrate is not shown.

5 Conclusions

Since the first international presentation of a transfer process for monocrystalline thin-film Si solar cells [BRE1997] the number of contributions to this field is rapidly increasing from one photovoltaic conference to the next. Although the history of layer transfer processes is rather short in Si photovoltaics, record thin-film efficiencies are being reported for layer transfer processed cells since 1998 [TAY1998, RIN2000]. This rapid development was possible because the fast knowledge available from microelectronics is fully applicable to the monocrystalline Si films. However the fabrication technology of the microelectronics industry will ultimately be too expensive for large-scale production. We therefore have to concentrate on the development of new low-cost cell processes and processing equipment that is particularly adapted to the specific requirements of the layer transfer approach. The prospects are good for low-cost thin-film Si solar cells from layer transfer processes.

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Monocrystalline Si Thin Film Solar Cells: A New Era for Thin Film Photovoltaics?

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Abstract: We present recent thin film solar cell results utilizing the transfer of monocrystalline Si films to a glass superstrate. Using a 23 μm thick Si film epitaxially grown on a 1.5 μm thick quasi-monocrystalline Si film, we achieve a conversion efficiency of 14% for a 4 cm^2 sized thin film solar cell on glass. In contrast to the limited performance of polycrystalline Si thin film solar cells imposed by the presence of grain boundaries, we expect processes based on the transfer of monocrystalline Si to result in thin film solar cell efficiencies in the range of 15 to 18% depending on process maturity and complexity. The transfer of monocrystalline Si films therefore opens a new avenue to an efficient and competitive Si based thin film technology.

Introduction

A number of new concepts based on the transfer of monocrystalline Si films to foreign substrates are presently being investigated. As a result of these approaches, efficiencies significantly exceeding 10% have been reported. An overview on the current status of Si thin film solar cells can be found in Refs. [1, 2].

In 1997, Brendel presented the so called Ψ -process that transfers a waffle shaped, monocrystalline Si film to glass [3, 4]. The process forms a porous Si film on top of a textured (100)-oriented Si wafer. The porous film acts as a seed for the growth of a few micron thick epitaxial Si film. During epitaxy, a waffle-like (100)-oriented Si film enclosed by (111)-oriented planes forms, which is subsequently separated from the starting Si wafer. Two-dimensional device simulation shows, that a solar cell efficiency in the range of 17 to 18% appears attainable with only 1 to 3 μm thin monocrystalline Si-films owing to superior light trapping [5].

Another approach, the so called *Epi-lift* [6] utilizes the formation of (111)-oriented crystal planes during near-equilibrium growth of Si using liquid phase epitaxy. No solar cell data have been reported yet. Due to the faceted Si surface, good light trapping properties are expected.

Sony Corp. presented the first transfer solar cell result based on a 12 μm thin, monocrystalline Si film with an efficiency of 12.5% [7]. A transfer approach termed SCLIPS [8] based on epitaxial growth on porous Si by liquid phase epitaxy was recently presented by Canon Corp. A first thin film cell device with an area of 0.2 cm^2 transferred from one Si wafer to another Si wafer resulted in a conversion efficiency of 9.5% [9]. Our institute investigates [10 - 12], independently of Sony, a similar approach and we currently achieve a confirmed cell efficiency of 14% by transferring a 24.5 μm thick monocrystalline Si film to a glass superstrate. For an overview on transfer processes for solar cells and microelectronic applications see Refs. [2, 13]. Applications of our technology for large-area electronics are outlined in Ref. [14].

Considering our latest results, we expect the performance of transfer solar cells to approach the performance of ribbon-based Si solar cells from Evergreen Corp. with a conversion efficiency of 16.2% [15] and Georgia Tech with 17.3% efficient cells [16] both using 100 μm thick Si ribbons.

1. Processing of thin films solar cells

The formation of porous Si, as required in our process, results from the anodic attack of HF-containing etching solutions on monocrystalline Si. This attack caves the compact material and thereby dissolves 20 to 90% of the Si within the thickness of the porous film. The remaining Si-skeleton consists of crystallites with a diameter of 10 to 50 nm and preserves the monocrystalline structure of the original crystal lattice. The current density used during etching, the HF-concentration of the solution and the doping of the wafer determine the morphology and the porosity of the porous Si film [17]. Switching the current density from low to high current enables the formation of a surface-near low-porous and a buried high-porous layer and hence allows the formation of almost arbitrary layered sequences.

High temperature annealing initiates a structural change in porous Si. The pores of the film with low porosity with a size of several 10 nm transform into voids with a size of 100 nm up to 1 μm depending on the morphology and the porosity of the starting porous Si film. Due to the presence of these voids, we termed the crystallized film *quasi-monocrystalline Si* (QMS). During the crystallization process, regions with high porosity transform into a separation layer that fixes the QMS-film to the substrate. Due to a low fraction of Si in the separation layer, this layer is mechanically weak and allows one to separate the QMS-film from the substrate. At the present stage of development, we have removed several QMS-films from a single Si wafer.

Figure 1 shows the device processing of transfer solar cells: After the formation of an epitaxial layer on top of a QMS-film, see Fig. 1a, the solar cell process starts with a shallow phosphorous diffusion that creates a sheet resistance of around 100 Ω/square . A drive-in at 1000°C forms a thin SiO_2 film of around 18 nm thickness for electrical surface passivation. For front contact formation, we evaporate Ti/Pd/Ag, and a mesa groove defines the active area of the cell. Plasma-enhanced CVD serves to form a SiN_x -film deposited from a mixture of N_2 and SiH_4 at a temperature of 380°C, see Fig. 1b. Films with a refractive index of around 2.1 provide effective anti-reflection properties for the silicon to glass interface. The transfer process itself, see Fig. 1c, includes three steps: (i) A 35 μm thick Ag-stripe is soldered to the busbar of the solar cell and serves as a connection to the emitter after the cell transfer. (ii) Deposition of an epoxy glue onto the glass allows one to attach the front-side of the cell to the transparent glass-superstrate. (iii) Mechanical force enables one to remove the wafer and reuse it for further process cycles. At the present stage of our investigations, we have not yet demonstrated the recycling of a single wafer throughout the whole processing sequence. The highly doped QMS-film is electrically contacted via evaporation of Al, see Fig. 1d. This process results in a good ohmic contact even at an annealing temperature as low as 110°C.

2. Thin films solar cells results

Table 1 outlines the cell parameters of transfer solar cells with an area of 4 cm^2 confirmed by Fraunhofer ISE, Freiburg. Cells processed as described above achieve an efficiency of 13.6%. The 14.0% efficient cell has two additional features compared to those discussed in the previous section: i) An antireflection coating on top of the superstrate glass consisting of a MgF layer reduces reflection losses, and ii) a point contacted rear side for reduced reflection losses on the back contact. These point contacts, however, do not contribute to a reduced recombination of minority carriers since they are placed on the highly doped QMS film.

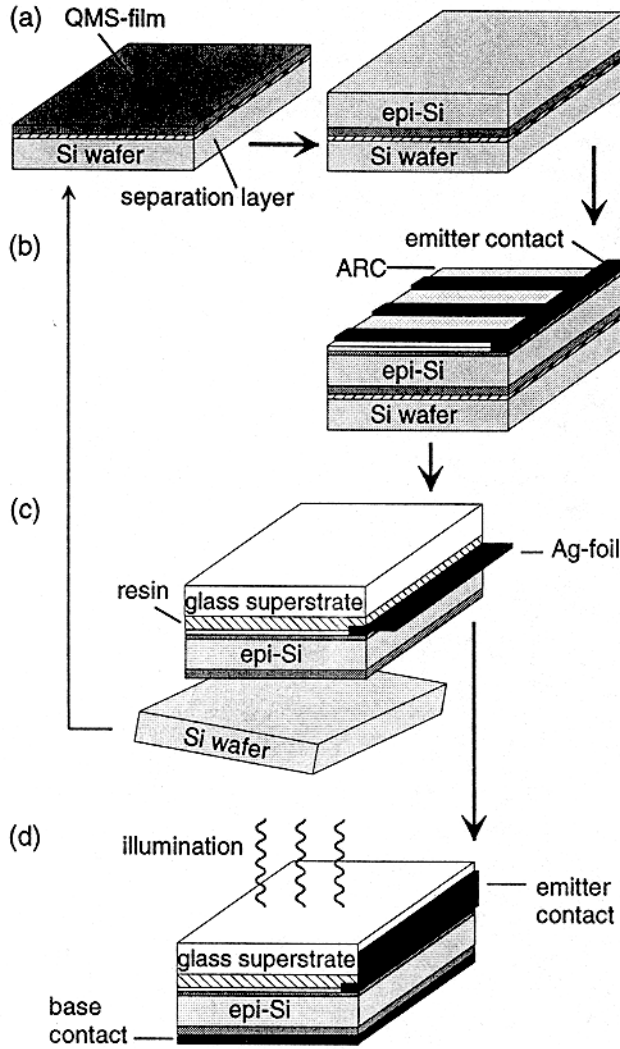


Figure 1: Thin film solar cell device processing sequence: a) Processing starts with the formation of a 1.5 μm thick QMS-film on a Si-wafer followed by epitaxial growth of a 23 μm thick absorber film. b) Cell processing by emitter formation using solid source diffusion, thermal oxidation and front contact grid formation. A SiN_x -film serves as an anti-reflection coating (ARC). c) A 35 μm thick silver foil is soldered to the emitter contact of the semi-finished device. After attachment to a glass superstrate, the wafer is consecutively separated from the thin film cell and may be reused for the next process cycle. d) Formation of a base contact by Al-evaporation. The cell is illuminated through the glass and therefore operates in a superstrate configuration.

Table 1: Confirmed cell parameters of transfer solar cells. Cells have a Si film thickness of 24.5 μm and an area of 4 cm^2 . For calibration, a shading mask with an area of 3.94 cm^2 is used.

V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)	rear contact	anti-reflection coating
633.4	26.69	80.6	13.6	full area	uncoated glass superstrate
634.2	27.33	80.5	14.0	point contact	MgF coating on glass superstrate

3. Conclusions and outlook

The high quality of our transferable monocrystalline Si films allows, up to now, an efficiency of 14.0%, the highest efficiency reported so far for monocrystalline Si thin film solar cells on glass. Device simulations for solar cells of the type described in this paper indicate an efficiency potential of 15 to 18%. For a detailed compilation of simulated efficiency see Ref. [11].

The success of monocrystalline Si transfer approaches will depend on the demonstration of i) high yield during multiple reuse of Si wafers, ii) successful upscaling, iii) use of simple

processing, especially in view of series connection of individual cells to modules, and (iv) low cost, high quality epitaxial growth.

Next to the approach presented here, the use of QMS-films without the involvement of epitaxial growth appears to be a particularly interesting and simple approach for transfer thin film solar cells. In view of the achievements coming from transfer techniques used for micro-electronics and the solar cell results presented here, it appears likely that we are indeed approaching a new era of solar cell thin film technology based on the transfer of monocrystalline Si films.

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MOLECULAR-DYNAMICS FOR SELF-INTERSTITIALS IN Si

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Abstract

Self-interstitials (Is) in Si are generated during ion implantation and processes such as oxidation or nitridation. They diffuse rapidly and interact with a range of defects and impurities. We calculate the static and dynamic properties of the isolated Is and I_n complexes with $n \leq 4$.

I. Introduction

The basic intrinsic defects in c-Si are the vacancy (V) and the self-interstitial (I). Is are not observed because their activation energy for diffusion in the presence of minority carriers is so low that they trap at shallow donors or H, form I_n precipitates, kick-out substitutional impurities such as B or C, recombine with vacancies, or diffuse to the surface before they can be observed[1].

Many sites have been proposed for the isolated I, including the tetrahedral or hexagonal interstitial sites[2], the bond-centered (BC) site[3], and a split- $\langle 100 \rangle$ structure.[4] However, recent ab-initio calculations favor the split- $\langle 110 \rangle$ configuration for the neutral I[5-11].

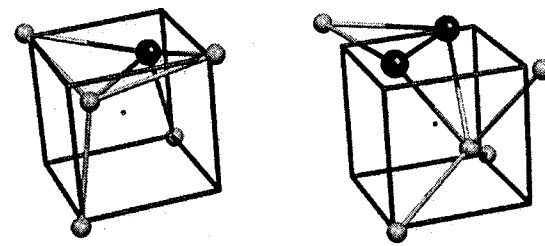
Several calculations of the structures of small I_n precipitates have also been performed. Rasband *et al.*[11] used empirical methods and proposed several structures for the di-interstitial I_2 . Arai *et al.*[12] also used empirical methods to obtain the structure of the I_4 aggregate. Lee proposed a di-interstitial model based on an EPR spectrum[13]. Coomer *et al.*[14] performed ab-initio density-functional calculations in H-saturated clusters for various structures of I_n aggregates, with $n \leq 4$. Finally, we reported[15] preliminary structures and properties for I_n aggregates on the basis of minimal basis-set, non self-consistent (Harris energy functional[16]), ab-initio molecular-dynamic simulations[17].

In this work, we report the results of fully self-consistent ab-initio MD simulations. The basis sets consist of linear combinations of atomic orbitals. Here, double-zeta plus polarization functions are used[18]. We perform simulated quenches to obtained the minima of the potential energy as well as constant-temperature runs. The host crystal is represented by periodic supercells of 64 and 216 host atoms (Harris functional calculations) or 128 host atoms (self-consistent calculations). The time step is 2.0fs. For details, see Refs.[18,19].

II. I_n aggregates: static properties

I^0 has a split- $\langle 110 \rangle$ configuration but the center of the split is shifted by about 0.7Å in the $\langle 001 \rangle$ direction. Metastable configurations exist. However, they transform into the stable one following high-temperature runs and quenches. Similarly, only one configuration of I_2 is thermally stable. It has the two Is bound to each other and aligned along a $\langle 110 \rangle$ direction. This can also be viewed as two Is bridging the same BC site. I and I_2 are shown in fig. 1.

Fig. 1: Lowest-energy configurations of the neutral I and I_2 complexes. The tetrahedral cube is shown and the dot in its center marks a perfect substitutional site. The self-interstitial(s) is (are) in black.



Two configurations of I_3 survive high-temperature runs followed by quenching. Both have the three Is forming an equilateral triangle in the $\{111\}$ plane. In the lowest-energy one (I_3^a), the center of the triangle is at a BC site, that is the three Is bridge the *same* Si-Si bond. In the higher-energy one (I_3^b), 1.7eV higher in energy, the three Is bridge *three adjacent* Si-Si bonds. These structures are compared in Fig. 2.

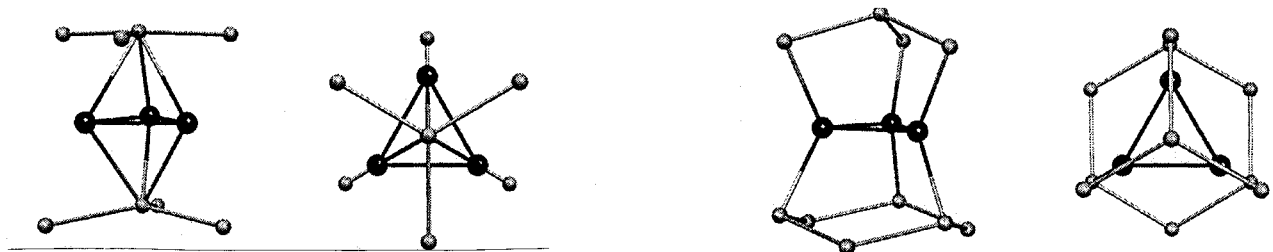


Fig. 2: Views of I_3^a (left) and I_3^b (right) perpendicular to and along the $\langle 111 \rangle$ axis.

The binding energy of the I_n complexes, defined from $I_{n-1} + I \rightarrow I + \Delta E_n$, are 1.7, 2.4, and 0.7eV for $n=2, 3$, and 4, respectively. Thus, I_3^a is the most stable of the small I_n complexes. The electrical activity associated with the various I_n complexes can be estimated by considering their energy eigenvalues. Deep 'gap' levels are associated with localized states while an empty 'gap' (as compared to the perfect cell) suggests no electrical or optical activity. The number and location of gap levels are not predicted accurately. An inspection of the energy spectra reveals that all the I_n complexes are electrically active. Their interactions with hydrogen are discussed elsewhere.[20]

III. I_n aggregates: dynamics

Because of the large amounts of computer time involved in constant-temperature MD simulations, most of our runs were performed with the Harris functional code. However, the key results were checked at the self-consistent level with double-zeta plus polarization basis sets. The longest of these calculations used 65 days of CPU time on a 56-processor Origin 2000 supercomputer. The same behavior is seen with both methods. Runs were repeated with different initial positions for the defect and at different temperatures. The results discussed below are reproducible.

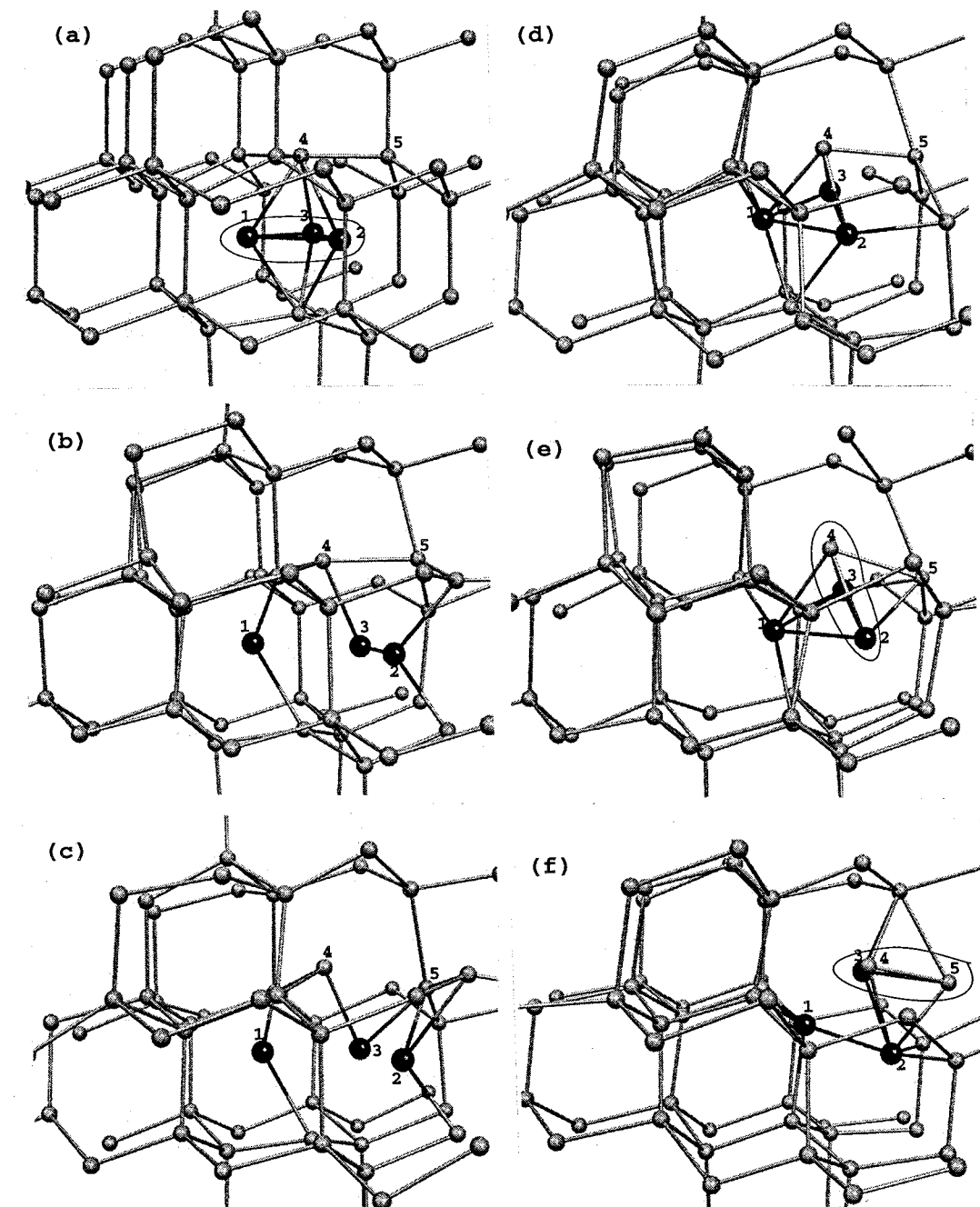
It is often assumed that *isolated* native defects are the fast-diffusing species and that aggregates are not. For example, monovacancies diffuse much faster than divacancies. When two vacancies form a divacancy (at a gain of about 1.6eV[21]), this energy must be overcome for dissociation to occur and monovacancies to diffuse again. Self-interstitials are different.

Runs at 1,000K with I or I_4 in the cell show nothing special: The Si atoms vibrate around their equilibrium position. However, I_2 and I_3^a diffuse with almost no activation energy. This is not associated with some strange initial velocity distribution. Were this the case, one would see a complex do one jump while the cell thermalizes then stop. Our longest simulations show see four or five successive jumps. The complex sometimes moves back one step then jumps again in another direction. As for I_3^b , the three Is continuously exchange position with each other, but the complex remains associated with the same tetrahedral cage (no diffusion).

Each diffusion step for I_2 or I_3^a occurs following one exchange process. The trick is that these two complexes involve a single BC site, with only two (host) Si nearest neighbors. The remarkable ease with which exchange occurs is caused by the fact that two (for I_2) or three (for I_3^a) self-interstitials join forces to displace the *same* host atom. An analogy would be to think of two or three muscular men working together to lift the same weight. As soon as one of the Is succeeds, the other two need very little displacement for the entire defect to be centered around a BC site adjacent to the original one.

At 1,000K, we observe two jumps in about 2.5ps, while at 77K, the same requires about 7ps. At 10K, no jump had occurred after 14ps. A plot of the potential energy vs. time as I_3^a diffuses at 77K reveals variations smaller than 0.3eV. This value is the *total* potential energy of the 67 Si atoms in the cell. Si atoms not involved with the diffusion vibrate around their equilibrium site and contribute to the total potential energy. Thus, 0.3eV overestimates the actual barrier for diffusion of I_3^a .

Fig. 3: Steps from a simulation at 1,000K. In (a), I_3^a (atoms 1-2-3) is quenched. In (b), (c), (d), an exchange takes place (atoms 1 and 4). In (e), 2.6ps after (a), one jump occurred and I_3^a consists of atoms 2-3-4. In (f), a second jump occurred: I_3^a now consists of atoms 3-4-5 following the exchange of atoms 2 and 5.



The rapidly-diffusing I_3^a complexes are attractive candidates as the building blocks of extended defects such as platelets. We are in the process of analyzing the dynamics of I_3^a precipitation. We are also calculating potential energies associated with various stacking structures of I_3^a 's.

Our calculations predict that neither I_2 nor I_3^+ can be seen experimentally: They diffuse much too fast and should react with defects or impurities before being detected. But I_3^0 appears to be stable. It shows no tendency to diffuse after some 10,000 time steps at 1,000K. It has been proposed[14] as the defect responsible for the W optical center. Our results are not in conflict with this assignment.

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DEPOSITED POLYCRYSTALLINE SILICON LAYERS ON MULLITE SUBSTRATES FOR SOLAR CELLS

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1. INTRODUCTION

Among the alternative approaches to bulk silicon based cells, there is the use of polycrystalline silicon thin films ($< 30\mu\text{m}$) on low cost substrates. Important issues in these developments are the choice of the substrate and the growth method since reasonably high growth rates and an overall reduction of the number of steps are essential in order to obtain a cost-effective process. As for the silicon formation, direct deposition on foreign substrates by chemical vapor deposition at elevated temperature ($>1000^\circ\text{C}$) and atmospheric pressure is suitable since it allows high deposition rates ($> 1\mu\text{m}/\text{min}$). Concerning the substrate, it should definitely provide a thermal expansion coefficient of approximately $4 \times 10^{-6} \text{ K}^{-1}$ in particular at high processing temperatures to avoid any peeling off the as-grown silicon layer. Additionally, the substrate has to present good physical and chemical characteristics for the deposited silicon layer and inhibits any out-diffusion of substrate impurities into the active layer during the deposition process. Thus, the option is limited to a couple of substrates such as graphite, high temperature glass, alumina (Al_2O_3), SiN_x , SiAlON and mullite ($3\text{Al}_2\text{O}_3\text{-}2\text{SiO}_2$). The advantages of insulating mullite substrates are that its thermal expansion coefficient can be precisely adapted to silicon, large scale production through tape-casting is feasible and allows a monolithic integration of modules. Furthermore, mullites exhibits high reflectivity, which is crucial for an effective optical confinement. However, few reports [1-4] concerned silicon on mullite because high-quality mullites are not commercially available. Therefore, they have been fabricated in laboratories [2,3] for this specific purpose.

Here we report on the deposition of $10\text{-}40\mu\text{m}$ thick polycrystalline silicon films on commercial and laboratory-made alumino-silicate substrates in a rapid thermal chemical vapour deposition (RTCVD) furnace. The as-grown silicon layers were analysed structurally and electrically to investigate their suitability for cell processing. The diffusion of contaminants from the mullite substrates to the layers were studied in order to assess the need of a barrier layer. The quality of the poly-Si/mullite based solar cells were investigated through the PV parameters and spectral response. The limitation factors for the obtained efficiency values are discussed. Improvement of the performances has been obtained through hydrogen passivation but more significantly by grain enlargement using the zone melting recrystallization (ZMR) technique.

2. EXPERIMENTAL

Three different types of mullite ($3\text{Al}_2\text{O}_3\text{-}2\text{SiO}_2$) substrates have been used for silicon deposition: commercially low-grade mullite (Kyocera, Japan), high purity sol-gel (LMPM, France) [2] and tape-casted (GEMPPM, France) [3] mullite. The main properties of such substrates are summed up in Table I. The mullites substrates differ mainly by the degree of porosity, purity and optical reflectance. The two first parameters are important for structural and electronic quality of the deposited silicon layer whereas the high reflectivity is a pre-request for an effective optical confinement.

The RTP-CVD reactor we use for Si deposition is a commercial stainless-steel reactor cooled with water, working at atmospheric pressure and using trichlorosilane (TCS) as a silicon gas source and trichloroborane (TCB) as a doping gas. The substrates are heated by 12 tungsten halogen lamps from the topside through a double quartz window cooled with oil. Cooling of the walls allows avoiding contamination of the growing film. Before deposition, the ceramic substrates were ex-situ cleaned in boiling HNO₃, DI water, IPA, and finally dried at 200°C. The depositions were carried out at temperatures ranging from 1000 to 1250°C for typical duration of 30 s to 5 min. The input partial pressure of TCS was set at 15% diluted in H₂.

Table I: Mechanical properties of the mullite substrates used in this work

	Silicon	M1 (Kyocera ^a)	M2 (LMPM ^b)	M3 (GEMPPM ^c)
Processing	-	Roll Compaction	Dry pressing of sol-gel	Tape-casting of Alumina-silica powder
Density	2,32	3,85	3,4	3,16
Max. T° [°C]	1410	1600	1550	1700
Therm. exp coeff. α [10^{-6} °C ⁻¹]	3,9	6-8,5	4.5	3,1-4,1
Porosity [%]				
Open	-	?	0	0
Total	-	15	< 5	2
Roughness Ra [μ m]	-	>1	0,5	0,53
purity	-	>90	99.9	99.7
Reflectance (%) at $\lambda > 800$ nm	-	45	80	80

^aKyocera, Japan

^bLMPM: Laboratoire des Matériaux et Procédés Membranaires, Montpellier, France

^cGEMPPM: INSA-Lyon, Villeurbanne, France

3. STRUCTURAL QUALITY OF THE DEPOSITED SI LAYERS ON MULLITE:

The microstructure of the poly-Si layer deposited on the mullite substrates in our RTCVD system is found to be heavily sensitive to the substrate temperature, input partial pressure of the precursor and the substrate material itself. The size of the crystallites attain their maximum with the utmost deposition temperature and reactant concentration due to the increased supply of adatoms to the growing structure and reducing the activation energy for a likely enhanced cluster mobility facilitating the growth of large grains.

Figure 1a gives the surface morphology of Si deposited for 5 min on M3 substrate at 1150°C. One can see a surface grain size distribution centred around 5-6 μ m. Maximum sizes of up to 30 μ m can be obtained according to temperature deposition or thickness, but small ones are always observed. These small grains can have a significant role on the electrical transport properties, as will be discussed below. The surface roughness of the as-deposited silicon acts as a natural surface texturation. The cross-section of such a layer is shown in Figure 1b. The layer thickness being 30 μ m means that deposition rates up to 6 μ m/min can easily be reached in our reactor. Figure 1b shows that the Si adheres perfectly on the substrate despite some residual surface porosity and surface roughness. The grain structure, as revealed by Secco-etching of polished cross-sections, appears columnar, with grains growing at the expense of others. This results in a quite large grain size distribution that broadens with layer thickness. X-ray diffraction carried out on these Si layers reveals that the grains are mostly <220> oriented. Similar results are obtained with M2 substrate. In contrast, deposition on the low purity commercial mullite substrates (M1) reveals an imperfect surface structure with voids. Additionally, a great amount of metallic impurities (i.e. Mg, Fe, Co) resulted in strong needles and whiskers formation and no

complete coverage of the substrate. In conclusion, merely mullite substrates with a low porosity and high purity can promote high quality growth of active Si layers.

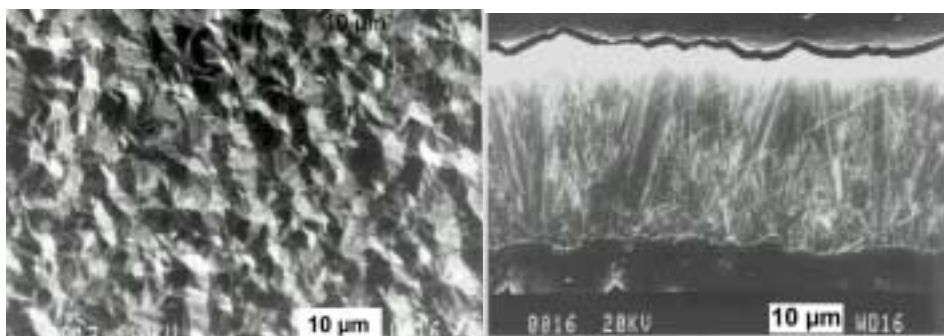


Figure 1. surface (a) and Cross-section (b) SEM photographs of a 30 μm thick Si layer deposited on mullite M3 substrate at 1150°C for 5min, 15% TCS in H_2 .

When we deposit Si at high temperature on a foreign material, an important concern is the possible contamination of the layer by solid diffusion of impurities (i.e. metallics) from the substrate [5]. We have probed the presence of the impurities by SIMS and DLTS (deep level transient spectroscopy) in Cz-Si samples which were in close contact to the mullite substrates and annealed in the RTCVD reactor at 1200°C during 2min under N_2 . Figure 2 gives the DLTS spectra for Si on M1 and M3 substrates. Much more peaks with high amplitudes are detected for Si on M1 compared to M3. This confirms the low purity of the commercial M1 mullite substrates. Although DLTS is unable to give the chemical signature of the detected point defects, activation energies and cross sections of the observed traps allow us to speculate that the main contaminants are Mg and Fe. Although the impurities should be under oxide form in the mullite material, the high porosity in M1 enhances their escape as hydrogen and chlorine from the precursor can easily penetrate through the material. Dense mullite material like M2 and M3 is therefore preferred.

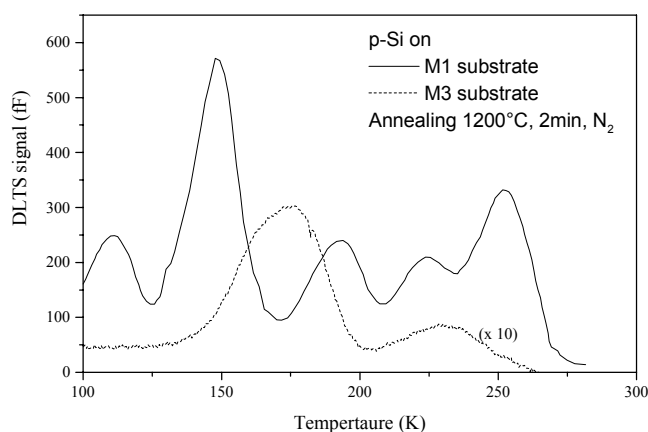


Figure 2. DLTS in Cz-Si on M1 and M3 mullites and thermally heated at 1200°C during 2min under nitrogen.

3. SOLAR CELLS : RESULTS AND DISCUSSIONS

Table II gives the illuminated I-V parameters of the best cells realised on polycrystalline Si-layers deposited on mullite ceramic, as well as on oxidised wafers (t-SiO_2) substrates. The latter substrate was used as purity references on which pc-Si layer is not affected by possible impurities originating from the substrate. With these reference substrates, best efficiency of 2.9 was obtained. In comparison, our best cell on dense mullite M3 substrate exhibits an efficiency of 2,8%. In order to evaluate the contamination issue, some mullite substrates were coated with AP-CVD SiO_2 . In this case, similar efficiencies (2,6%) were obtained, thus showing that the

cells so far are not affected by impurities but rather by the presence of the crystallographic defects.

Whatever the substrate is, the performance is limited primarily by the poor V_{oc} (< 400 mV) and accordingly by low FF ($< 0,6$). This fact has been reported by many authors for p-n junction solar cells made in fine-grained polysilicon [6]. The analysis of the I-V curves revealed that this was due to a very large recombination current. The ideality factors were reported to be close to 2 over the whole characteristics. It is likely that the recombination current is generated in the space charge regions along the junction as well as [7] in the smallest grains of the distribution that are completely depleted of mobile carriers, either by interface states at grain boundaries, or by the phosphorus-dopant spikes diffused along grain boundaries [8]. The hydrogenation step is found to strongly improve the quality of the cell but not enough.

A typical internal quantum efficiency (IQE) curve measured on fine-grained pc-Si cells is shown on figure 5. the IQE curve between 400 and 800 nm can be interpreted as being dominated by the emitter and space charge regions rather than by the base. The hump beyond 820 is attributed to light reflected by the substrate but absorbed and collected at the cell surface. This means that most of base thickness does not contribute to the collected current because of a high recombination of carriers generated in the base: the electrically active region of the device is mainly the near emitter region [9].

Increasing the grain size from micrometers to millimeters by zone melting recrystallization (ZMR) of pc-Si layers onto mullites yields to much better PV parameters [10] as given in Table II. The internal quantum efficiency (EQE) curve for such cell shows high response for wavelengths above 600 nm. Especially, the optical confinement offered by the mullite's diffuse reflection becomes fully exploited. Short circuit currents up to 26.1 mA were measured, slightly higher than that mentioned in [11] and obtained on similar structure.

Substrate	Film thick. [μm]	Hydr.	J_{sc} [mA/cm^2]	V_{oc} [mV]	FF	η [%]
p+ sc-Si	25	-	29.2	638	75	14
t-SiO ₂		Yes	14.1	350	58	2,9
Mullite	15	Yes	12.8	368	59	2,8
Coated mullite	15	Yes	12.6	348	58	2,6
		No	10.4	249	46	1,2
With ZMR	49	Yes	23.8	525	66	8.2

Table II. Illuminated I-V parameters of thin-film Si solar cells on mullite M3 substrates and compared to that on thermally-oxidized Si and epitaxial Si pn p⁺-Si.

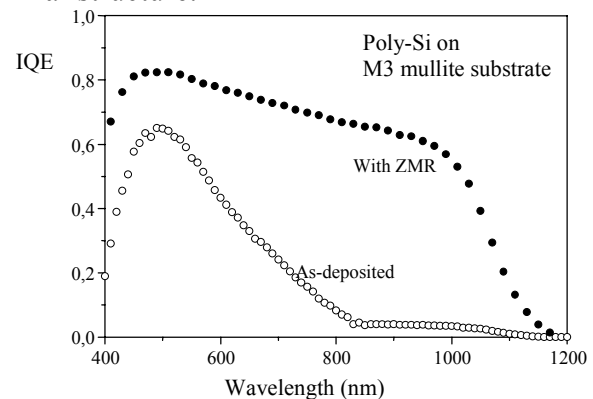


Figure 5: Internal Quantum Efficiencies of as deposited or ZMR treated pc-Si cells on mullite M3 substrates.

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Characterization of Electrically Active Dislocations in EFG Silicon Using Scanning Room-Temperature Luminescence

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Abstract

Scanning room-temperature photoluminescence was used for diagnostics of polycrystalline wafers to study the electronic properties of high-quality of solar-grade material. The intensity of a “defect” band at 0.8eV positively correlates with dislocation density measured using a light scattering method. We also found that the defect centers are localized in regions with a high elastic strain field.

Introduction

We report here on photoluminescence (PL) and stress mapping of recombination centers in high recombination regions of mc-Si wafers. These regions limit solar cell performance, and their monitoring, characterization and reduction is a primary goal in the search for approaches to achieve high cell conversion efficiencies. We present experimental evidence that low recombination regions are characterized by an intense “defect” PL band, which we associate with electrically active dislocation networks.

Experimental

Materials used in this study were boron doped mc-Si wafers up to 10 cm x 10 cm area and approximately 300 μm thickness grown by Edge-defined Film-fed Growth (EFG) technique. Some EFG wafers were subjected to solar cell processing steps and tracked by the PL method. The PL spectra and PL mapping were performed using setup described previously [1-3].

In the polarization study, infrared Polaroid film was used as the linear polarizer. The film was mounted on a 360⁰ rotary holder and the polarization plane was aligned to EFG crystal grain boundaries, which are easily viewed on the crystal surface.

To correlate the PL map with the distribution of extended crystal defects, a mapping of the dislocation density in mc-Si wafers was obtained with a PVScan-5000 photovoltaic analyzer, which employs a light scattering method [4].

For scanning measurements of the residual strains, we adopted a linear polariscope technique [5]. The intensity of the optical transmission was measured in a spectral region of the transmission window where Si is transparent, near $\lambda=1.3\mu\text{m}$. Infrared linear polarizers were oriented with respect to a pre-selected crystal direction, such as a grain-boundary in mc-Si. The polarization intensity, I , measured at selected orientations of the polarizer and analyzer, depends on the optical retardation parameter δ , which in turn is directly related to the value of the residual elastic strain. Two transmitted intensities of the polarized light are measured: one with polarizer and analyzer parallel to each other, $I_{\parallel} = I(\chi=0)$, and the second when the polarizer is rotated 90⁰ and orthogonal to the analyzer, $I_{\perp} = I(\chi=\pi/2)$. We could estimate quantitatively both the optical retardation, δ , and the direction of the principal stress angle, ψ . As the last step of the analysis, two strain components, $|e_{zz}-e_{xx}|$ and $|e_{xz}|$, can be

calculated [4]. The first term represents a difference in tensile strains along crystallographic Z and X directions, while the second term is the shear strain component between Z and X.

Results and Discussion.

The PL spectrum at room temperature is generally composed of two bands in as-grown and processed mc-Si wafers (Fig.1). The high-energy maximum at 1.09eV corresponds to band-to-band emission (I_{bb}) caused by phonon-assisted recombination of bound and unbound free electrons and free holes [6]. A second broad band at lower energies, with the maximum at about 0.8eV, is referred here as the defect band (I_{def}).

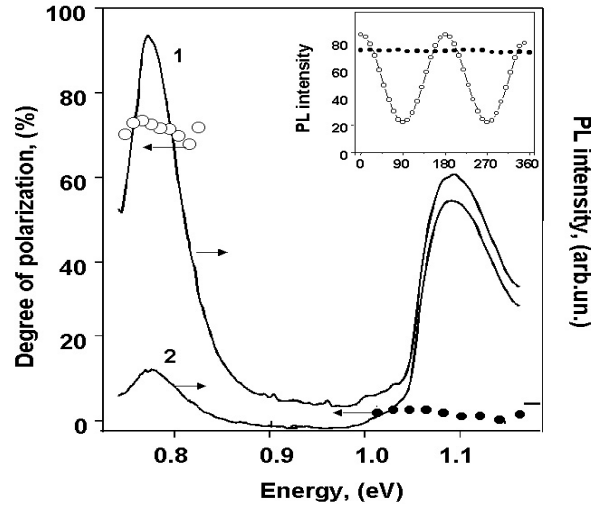


Figure.1. Two PL spectra an EFG wafer measured in polarized light at orthogonal orientation of the polarizer corresponding to (1) maximum $\chi=0^\circ$ and (2) minimum $\chi=90^\circ$ intensity of the defect PL angular dependence as shown at the inset. Circles represent spectral dependence of the polarization degree for defect PL (open circles) and band-to-band PL (solid circles).

Inhomogeneity in the electronic properties of EFG wafer gives rise to distinct high and low lifetime regions [1-3]. An interesting property of low lifetime regions is an intense PL band with a maximum at about 0.8eV and a half-width of ~ 70 meV. The intensity of the “defect” band is highly inhomogeneous across the wafer. The PL maximum of the “defect” band varies between 0.76 and 0.81eV, we tuned the spectrometer to the “defect” band maximum and scanned the wafer to map the distribution of “defect” band intensity (Fig.2.b).

The topography of the I_{bb} distribution is very similar to that of the lifetime. We have documented previously that a linear relation between I_{bb} and lifetime is obtained for both as-grown cast and EFG mc-Si from a point-by-point comparison of maps of both quantities across the wafer [3]. This confirms that the band-to-band PL is sensitive to recombination lifetime and can be used as a complimentary technique to lifetime mapping to characterize photovoltaic mc-Si material.

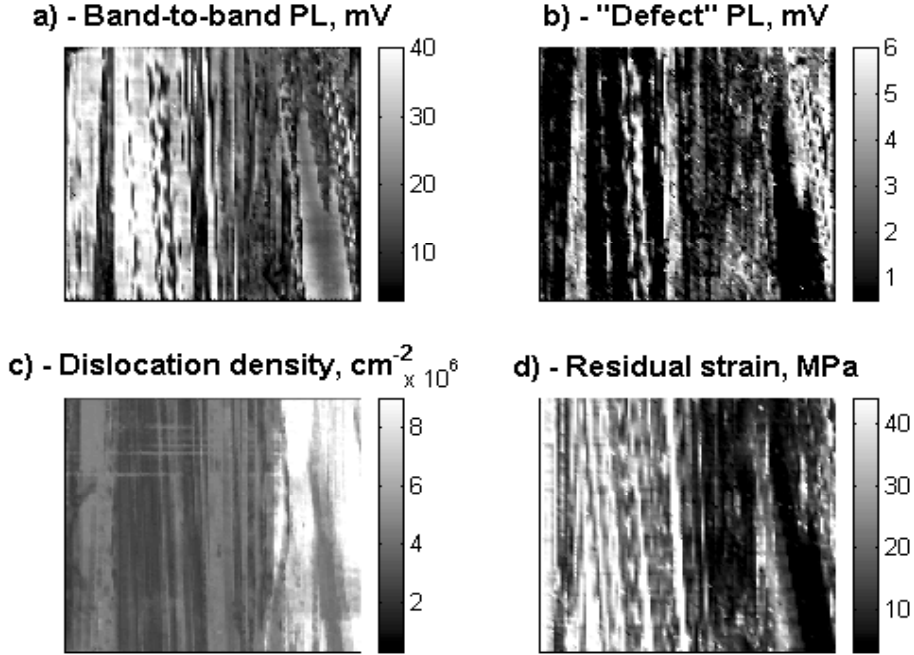


Figure 2. Maps of band-to-band PL (a), defect band (b), dislocation density (c) and residual strain (d) in an unprocessed EFG wafer. The mapped area are $10 \times 10 \text{ cm}^2$.

We reported previously for EFG wafers, the dislocation density correlates with variations of the defect PL band [1-3]. The 0.8eV PL band is observed most consistently in areas with dislocation density $\sim 5 \times 10^6 \text{ cm}^{-2}$ (Fig.2.b,c). However, some dislocated areas in the EFG wafer do not show a defect peak. We conclude that, although the “defect” PL band originates in areas with high recombination activity and increased dislocation density, there are other factors which contribute to produce the defect PL peak.

An interesting property of the 0.8eV PL band is a linear polarization of the “defect” band. Fig.1 shows two PL spectra measured with a linear infrared polarizer oriented in two orthogonal directions of the polarization plane. These two directions were selected at a maximum and minimum of I_{def} versus azimuth angle of the polarizer, as depicted in the insert in Fig.1. In contrast to the defect band, the intensity of band-to-band PL measured at exactly the same point on the wafer is unaffected by the polarization direction, i.e., this amplitude is unpolarized. We find in EFG samples that the maximum intensity of the defect PL band is observed when the polarization direction is perpendicular to the nearest grain boundary. We also measured the degree of polarization in other regions of the same EFG wafer, and found that it varies between 58 and 72% (Fig.1). This is a very high degree of polarization, and corresponds to strongly polarized optical transitions, a situation which is only observed in Si single crystals subjected to uniaxial stress [7]. This suggests that the internal stress field due to crystallographic defects - grain boundaries and dislocations - is the source of the anisotropy revealed by this polarization in the PL defect band.

To clarify this situation, we performed a polarization transmission study of the strain distribution in EFG wafers using scanning linear polariscopy [5]. The strain maps

were compared with a distribution of the defect PL band intensity on the same wafer using an identical optical alignment.

A typical result of strain field mapping is presented in Figure 2.d. The strain field component has a linear geometry and mirrors the orientation of the nearby grain boundary. In mapping the entire wafer, we found regions with stress as high as 35 MPa. The defect PL band distribution has a distinctive linear distribution of maxima in the vicinity of the high stress areas, as seen in Figure 2. The maximum “defect” peak signals come from regions located on both sides of the stress concentration, in some cases within a few hundred microns from the area of maximum stress [3]. It may be significant that the defect PL maxima do not directly coincide with the bands of maximum stress, but are adjacent to these stress areas. The defect centers responsible for the 0.8 eV PL band appear to be strongly affected by the anisotropic stress field of crystallographic defects, which leads to the high degree of polarization observed for this band.

Conclusions

In summarizing the properties of the 0.8 eV defect PL band in mc-Si, we conclude that its luminescence originates from electrically active dislocations, which interact with defects. It is very likely that oxygen precipitates and heavy metals are mainly involved; however, other impurities such as C and defects formed from self-interstitials or their clusters may also contribute. The defect centers are localized in regions with a high elastic strain field. We have independently assessed the elastic properties of the mc-Si and measured the degree of linear polarization produced by the strain field.

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LOW-TEMPERATURE CHLORINE-FREE PROCESSES FOR PURE SILICON FEEDSTOCK PRODUCTION

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I. Introduction and Background

The photovoltaic (PV) method of generating electricity from sunlight has attracted growing public attention. The many advantages of photovoltaic solar energy include no moving parts, no pollution, no noise, long (30-year or more) solar module lifetime, and no need for fuel delivery. In addition, PV generating systems are modular: the system size can be easily expanded as the need increases. A PV system can have an electricity generating capacity as small as a few milliwatts—as in calculators and watches—or as big as hundreds of megawatts (MW)—as in centralized power stations.

Photovoltaics have been the basic source of energy aboard space vehicles for more than 40 years, and the use of PV solar technologies on earth is growing rapidly. For example, building-integrated PV applications have increased rapidly. Recently, Germany has successfully completed the "1000 Roofs" program, with each roof equipped with a PV system generating 2 to 3 kW of peak power. The European Commission, in a white paper entitled «Energy for the Future: Renewable Sources of Energy» [1], calls for a hundred-fold increase of PV applications—from some 30 MW presently to 3 gigawatts installed in the European Union, plus an equivalent amount of export. The United States has also announced its own program, the «Million Solar Roofs Initiative» [2]. Japan's plan for building-integrated PV is similar to these scales.

On the threshold of the 21st century, the annual worldwide production of PV solar modules and systems has reached well over 100 MW. Average annual worldwide PV market growth has been around 15% for the last 12 years, with 1997 growth posted at 42%. The growth rates of the PV industry in the last 3 years have mainly been limited by the availability of low-cost polysilicon feedstock material. About 90 percent of the world PV cell manufacturing is based on high-purity polysilicon as the starting material. The other 10 percent is mostly based on amorphous silicon thin-film solar cells, which are produced using gaseous compounds of silicon with hydrogen. The minimum average consumption of polysilicon is 10 tons per 1 MW of power. According to available data, the worldwide usage of polysilicon for solar-cell manufacturing was about 1200 tons in 1995. However, at this time, there is no factory production of polysilicon specifically for the solar industry. The source of solar-grade silicon is mainly the rejected material from the semiconductor electronics industry, which amounts to about 10% of the polysilicon material used by the electronics industry.

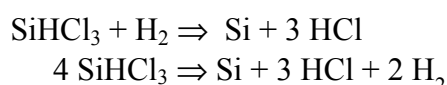
The annual increase in the world production of electronic-grade polysilicon has been between 10% and 12% annually. The annual increase in demand for solar-grade polysilicon is also high (about 15% for the last 12 years), especially in recent years (more than 40% in 1997). Starting in 2003, the shortage of solar-grade polysilicon has been the main factor limiting the growth of the PV solar-cell industry [3]. And this problem will get worse unless we build facilities dedicated to producing solar-grade polysilicon. One can further reduce the risk of the investment of producing polysilicon by building factories that can produce polysilicon of both electronic and solar grades, depending on the market demand.

II. Literary Survey

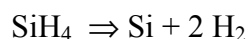
In spite of great progress in elaboration of the new semiconductor materials silicon is the basic electronic material as before. In accordance with increase of the element density and fast response of the integral circuits the requirements to the purity and homogeneity of silicon are increased too. The main demand to the purity of raw silicon is decrease of content of boron lower than $1 \cdot 10^{13} \text{ cm}^{-3}$ and oxygen and carbon lower than $1 \cdot 10^{15} \text{ cm}^{-3}$. At present time two main methods of high purity (semiconductor grade) silicon producing are known:

- 1) with using of trichlorsilane SiHCl_3 ;
- 2) with using of monosilane SiH_4 .

When producing of silicon from trichlorsilane the reactions of hydrogen reduction and thermal decomposition of trichlorsilane are proceeded:



Under these reactions the SiCl_4 and HCl are formed as the by-products that leads to (i) - decrease of silicon output; (ii) - pollution of silicon with the bad impurities in result of corrosion of the reaction chamber and (iii) - arising of the ecological problems. The advantage of trichlorsilane is easiness of it's producing by direct interaction of large-grain powder of metallurgical silicon with hydrogen chloride and the secondary yielding SiCl_4 can be returned to processing using the distillation without considerable expenditures. Moreover trichlorsilane is easily available as it is produced in great amounts for manufacturing of the organosilicon polymers. However, it is difficult to produce super purity silicon with using the trichlorsilane. For producing of such silicon more preferable way is using of monosilane technology completing of thermal decomposition of monosilane in accordance with the reaction:



The main advantages of monosilane technology are following:

- ☐ thermal decomposition of monosilane is proceeded at relatively low temperature (approximately 850°C instead of 1100°C for trichlorsilane) and less energy consumption;
- ☐ the chemically aggressive agents (hydrogen chloride, chlorsilanes, etc.), decreasing the silicon purity, are absent among the reaction products;

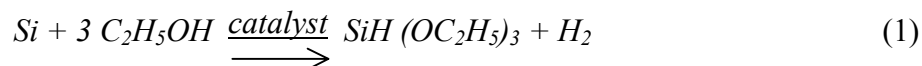
- purification of monosilane from most of the bad impurities at other equal conditions is more effective in consequence of considerable difference of physical and chemical properties of monosilane and impurity compounds;
- like the silicon the monosilane and its mixtures, necessary for thin film technology of producing of semiconductor articles and fast growing manufacturing of the solar modules on the base of α -Si, are the commercial products.

However, many known methods of silicon producing through monosilane stage are complicated and the necessary expenditures are greater as compared with using of trichlorsilane. So for purification of monosilane by distillation at low temperature the cooling by liquid nitrogen and helium is required that strongly increases the basic cost of such silicon. Moreover, the known methods of monosilane producing are enough complicated as compared with trichlorsilane and high purity monosilane for semiconductor industry is expensive. That is why the using volumes of monosilane are limited and it is used only production of super purity silicon for growth of the single crystals by floating zone method.

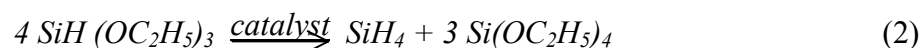
III. Proposal for Polysilicon Feedstock Facility

We propose to build such a manufacturing facility for polysilicon feedstock, using a chlorine-free technology and using metallurgical-grade silicon and alcohol as the starting materials. The basic processing stages are the following:

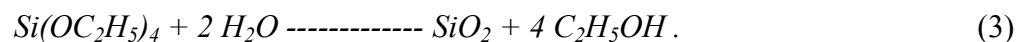
1. The reaction of silicon with alcohol proceeds at 280°C in the presence of a catalyst in ambient of high boiling solvent:



2. The disproportion (i.e., simultaneous oxidation and reduction) of triethoxysilane in the presence of the catalyst will lead to the production of silane and tetraethoxysilane:

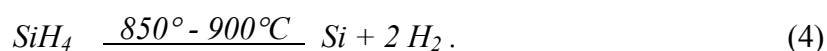


3. Dry ethanol and such secondary products as high-purity SiO_2 or silica sol (colloidal silica) can be extracted by hydrolysis of tetraethoxysilane. The alcohol will be returned to Stage 1.



Principal scheme of this three processes is illustrated by Fig. 3-5.

4. Silane is decomposed pyrolytically to pure silicon and hydrogen at a temperature of about 900°C :



The purity requirements for solar-grade silicon are not as high as those for electronic applications. Thus, the silane will undergo a simplified cycle of purification, and at Stage 4 the less expensive and less energy-consuming process of a "fluidized bed reactor" can be used, instead of the well-known

"Siemens Process." Figure 6 shows the basic diagram of processing metallurgical-grade silicon into silane, pure silicon feedstock, and other useful by-products.

According to this proposed method, alcohol that was not used in the reaction with metallurgical silicon, is returned for interaction with silicon. Obtained concentrated mixture of alcoxysilanes is catalytically disproportionated at temperature $-20 + 40^{\circ}\text{C}$ within 1-50 hours with extraction of gasified monosilane, prepurified by absorption of admixtures, the tetraethoxysilane is extracted from liquid products of disproportionation after addition of organic alcohol. Tetraethoxysilane is subject of full hydrolysis with processing commercial colloidal silica sol and organic alcohol, which is directed to reaction with silicon after dehydration by tetraethoxysilane.

IV. Advantages of Our Proposed Method

The unique advantages of the proposed method to produce pure polysilicon feedstock are the following:

- The initial materials, such as metallurgical-grade silicon and alcohol, are available in essentially unlimited quantities at relatively low cost. World production of metallurgical silicon has reached the level of 1,000,000 tons per year, and only 1% of it is used to produce silicon for electronics.
- Chlorine compounds are not used, and the process is ecologically safe.
- The reaction products do not interact with the reactor's walls, and the reactors may be built using typical construction materials, thus minimizing pollution of the finished products.
- The chemical reactions are connected with the silicon only and proceed with almost no precipitation of foreign impurities in silicon. That is why the cost of purification of silicon is decreased.
- All processing proceeds under normal pressure, and the maximum temperature does not exceed 300°C .
- Net wastes of metallurgical silicon less than 4.5 percent. Practically all processing wastes are used to produce the valuable by-products.
- The main high-purity products are silane, pure silicon feedstock (solar or electronic grade), silica sol, silicon dioxide, and tetraethoxysilane. The industrial demand for silica sol is increasing rapidly, now exceeding an annual level of 23,500 tons (corresponding to the total productivity of 1000 ton/year of the silicon feedstock).
- The process can easily be controlled to produce various products like silane and silicon feedstock (electronic or solar grade).

V. Characteristics of the Basic Production

Silane is produced in the pure state or in a mixture with argon under pressure. The silane purity exceeds 99.999 percent. Silane and its gas mixtures are suitable for forming thin layers of silicon structures in various semiconductor devices, including integrated circuits and solar cells. Semiconductor-grade polysilicon is produced using the Siemens process. In this process, a silicon-containing source gas is thermally decomposed on a heated silicon seed rod. High-purity polysilicon feedstock with resistivity above $300\ \Omega\text{-cm}$ can be produced. For lower costs, solar-grade polysilicon feedstock can be produced by silane pyrolysis using a fluidized bed reactor. Energy consumption for this process is lower ($< 100\ \text{kWh/kg}$) than for the Siemens process. The silicon produced is in the form of fine granules that can be used to form tablets. Silane does not require a complete cycle of refining for solar-grade polysilicon manufacture.

Processing of polysilicon feedstock to monocrystall Si by Czochralski growing method gives solar grade Si in granules form and electronic grade Si in ingot form. If multiple zone meeting and the grow of monocrystall Si in float zone are used, the high resistivity monosilicon with specify resistivity more than 1 kΩ-cm is obtained.

The results of analysis of high pure silicon specimens presented by GNIChTEOS at exhibition-collection of substances of ultra purity in 1990

Impurity	Content, % at.		Impurity	Content, % at.	
	Ingot №54-1	Ingot №54-2		Ingot №54-1	Ingot №54-2
Ag,Co,Ca, Zn,Mo, Pb, Th	$<1 \cdot 10^{-10}$	$<6 \cdot 10^{-10}$	Br,Cr,Lu,U,Z n	$<2 \cdot 10^{-9}$	$<4 \cdot 10^{-9}$
Al,B,Bi,Cl, F, I, Nb, P, Rh,Tc	$<3 \cdot 10^{-6}$	$<5 \cdot 10^{-6}$	Ca,Ge,Hg,Mg ,O,Os, Pb,Pd,Pt,S,Tl	$<1 \cdot 10^{-5}$	$<3 \cdot 10^{-5}$
As,Cs,Hf, La,Sm,Ta, W,Au	$<1 \cdot 10^{-11}$	$<4 \cdot 10^{-11}$	Ir,Re,Sb,Sc	$<1 \cdot 10^{-12}$	$<7 \cdot 10^{-12}$
Ba,Cd,Ce,D y,Fe, K, Mn,Na,Ni,S n,Ru,Se	$<1 \cdot 10^{-8}$	$<5 \cdot 10^{-8}$	Sr,Te,Zr	$<3 \cdot 10^{-7}$	$<6 \cdot 10^{-7}$
Cu	$<9 \cdot 10^{-10}$	$<9 \cdot 10^{-10}$	C	$<4 \cdot 10^{-4}$	$<4 \cdot 10^{-4}$

Specific resistance of monocrystalline silicon produced by crucibleless zone melting (5÷8 runs) reaches more than 10000 Ωcm and shelf life of minority charge carriers is no less than 1000 μs. This demonstrates the low content of electrical active impurities in PCS. Such silicon is suitable for manufacture of IR-detectors and of nuclear radiation detectors.

Monosilane and gas mixtures of monosilane with hydrogen and argon are widely used for manufacture thin layer silicon structures in different electronic parts including integrated circuits, solar modules and the like.

VI. Characteristics of By-Products

Tetraethoxysilane is a valuable product widely used in different areas of new engineering for manufacturing quartz glass and optical fiber materials, special optical glasses, and for forming dielectric films.

Colloidal silica sol is analog of colloidal silica "Ludox" (by Du Pont), "Syton" (by Monsato). Silica sol is product of condensation of polysilicon acids—represent stable dispersion, consisting of water and amorphous silicon dioxide particles with a diameter of 5 to 100 nm and specific surface-area of 270 to 550 m²/g. The contents of silicon dioxide in silica sols can reach 50 percent. The basic applications of silica sols include:

- binding substance for exact casting in metallurgy
- manufacturing of heat insulator materials with increased durability
- hardening fabrics in textile industry
- manufacturing of strengthened concrete

- manufacturing of radio-transparent composition materials.

Colloidal silica sols also find applications as binding and extender in different ceramic products, coatings, forms for casting, production of special glasses, cement, lacquer-paint coatings; as raw material for adsorbents, catalysts, and photosensitive materials; for increasing the ability to adhere and to prevent sliding; and for treating wood, cardboard, and fabrics.

The annual world total demand of silica sols exceeds 100,000 MT. The price of silica sol is about \$1-2 per kg on world markets. The need for tetraethoxysilane is hundreds times less, the need for clean SiO_2 is tens times less.

Pure silicon dioxide is widely used to manufacture high-quality quartz products and to grow crystals of piezoelectric quartz for manufacturing highly stable quartz resonators used as the basic elements for frequency selection.

The proposed technology allows us to use about 95 percent of the initial silicon.

X. Some Cost and Sales Estimates

Table 2 gives rough estimates for the cost of silicon to be produced by this process for the pilot and commercial scale.

Primary Cost of Producing 1 kg of Silicon Feedstock in U.S. Dollars at Production Scale

Category	Table 2 Production Scale	
	1 ton/year (pilot plant)	1,000 ton/year
1. Raw materials	13	13
2. Transport and supply	1.3	1.3
3. Energy expenditures	50	10
4. Salary	10.1	1.1
5. Taxes and insurance	4.5	0.5
6. Depreciation and maintenance of equipment	4.4	0.9
Total:	83.3	26.8

Manipulation and Control of Nucleation and Growth Kinetics with Hydrogen Dilution in Hot-Wire CVD Growth of Poly-Si

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ABSTRACT

We systematically explore the relationship between gas-phase kinetics and film microstructure in the hot-wire CVD technique using diluted silane (1% in He) and additional hydrogen. Using a wire temperature of 2000°C, films were grown on Si (100) at 300°C using 1 mTorr SiH₄ and 99 mTorr He at H₂ pressures from 0-100 mTorr. Transmission electron microscopy and atomic force microscopy measurements indicated that continuous microcrystalline films had a columnar grain structure and that grain size increased from 40 nm using SiH₄/He to 85 nm using SiH₄/He/H₂ with 20:1 H₂:SiH₄ ratio due to the etching of Si by atomic H. Etching rate measurements using a quartz deposition monitor show that, under the current deposition conditions, a transition from net film growth (0.17 nm/s using only SiH₄) to net etching occurs at a H₂:SiH₄ ratio of 80:1. The effect of atomic H on the nucleation density during the initial stages of growth has also been investigated, revealing a sublinear dependence of nucleation density with time and a decrease in nucleation density with increasing H₂ dilution. High deposition rate growth with no H₂ dilution has been achieved on a low-density array of seed nuclei produced using high H₂ dilution.

INTRODUCTION

Hot wire chemical vapor deposition (HWCVD) is an attractive method for growth of polycrystalline silicon thin films for application in thin film polycrystalline silicon photovoltaics [1,2]. A key issue is to identify growth conditions that enable the largest possible grain size at a given growth temperature with low intragranular defect density. Hydrogen is known to play a critical role in the development of a crystalline microstructure in both polycrystalline [3, 4] and epitaxial [5] films grown by HWCVD at low temperatures. The role of atomic hydrogen produced by the wire in the etching of amorphous Si and small crystalline nuclei and its effect on the resulting film microstructure are investigated.

EXPERIMENT

All experiments were performed at pressures of no higher than 1×10^{-6} Torr. A 0.25 mm diameter W wire was resistively heated to 2000°C and positioned at a distance of 2.5 cm from the substrate. The wire radiatively heated substrates of 100 nm SiO₂ on Si to 300°C. H₂ dilutions are referenced to 1 mTorr of SiH₄ in 99 mTorr He; all gases used are ultrahigh purity. A translatable shutter between the wire and substrate enabled several growth experiments at identical gas ambient and wire temperature on each substrate at low Si coverage, and also provided a definite starting and ending point for film growth.

RESULTS

The net Si growth rate was measured using a quartz crystal oscillator located at the substrate position with H_2 dilution between 0 and 150:1. The oscillator was actively cooled during the measurements to a surface temperature of approximately 250°C. As seen in Fig. 1, the net growth rate decreases with increasing H_2 partial pressure, which was attributed to Si etching by atomic H. In a separate experiment, the SiH_4 flux, measured at the same H_2 dilutions with a differentially-pumped quadrupole mass spectrometer, with its orifice located at the substrate position, was observed to increase with the addition of H_2 . The increase was attributed to atomic H etching Si species from the chamber walls and recombining with these species in the gas phase. A transition from net growth to net etching of the amorphous Si grown on the quartz oscillator is observed with the addition of 80 mT H_2 . Since growth of crystalline Si was observed on SiO_2 substrates even at 80:1 H_2 dilution, the transition to etching most likely occurs at a higher hydrogen dilution due to a slower hydrogen etch rate for crystalline Si than amorphous Si [6]. Transmission electron microscopy (TEM) of films grown on SiO_2 substrates confirmed that, at a H_2 dilution of 20:1, Si films are fully polycrystalline; no initial amorphous layer is observed during film growth due to this etching process.

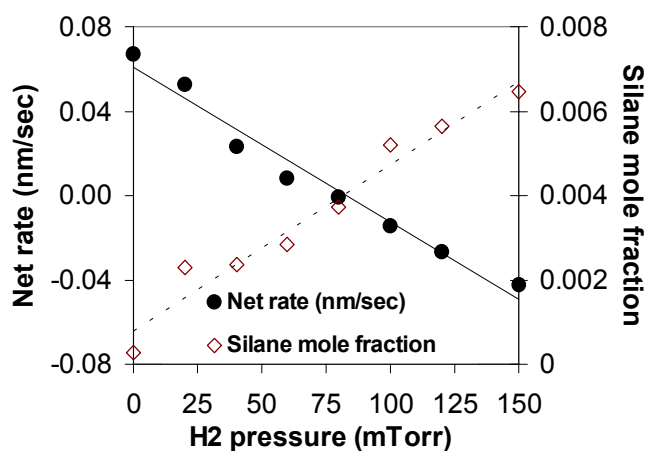


Figure 1. Net deposition rate and SiH_4 flux, as a function of H_2 dilution.

The nucleation density at low Si coverage on a 100 nm thick SiO_2 layer was determined using atomic force microscopy (AFM), as illustrated in Fig. 2, for H_2 dilutions between 0 and 80:1 in the region nearest the wire. As seen in Fig. 3, the nucleation density increased sublinearly with time, and was highest for no added H_2 , decreasing with H_2 dilution. The measurements of nucleation density are consistent with the AFM measurements in Fig. 4, which indicate an increase in grain size in thick, continuous films from 40 nm with no H_2 dilution to 85 nm at an H_2 dilution of 20:1. The nucleation rate is initially high until a critical density of nuclei is reached, at which time the nucleation rate is sharply reduced and grain growth begins.

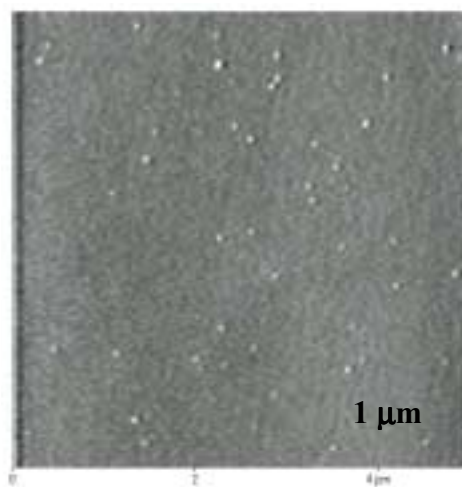


Figure 2. AFM image of HWCVD film grown at 20:1 H_2 dilution for 90 s, illustrating the nucleation phase. Bright features are 35 nm in height.

To determine the role of atomic hydrogen etching in the growth process, an SiO₂ substrate was exposed to 60 mT H₂ for 20 minutes, after which growth was allowed to proceed with an undiluted silane mixture. The resulting nucleation densities shown in Fig. 3 were similar to those for undiluted growth without previous H₂ exposure, suggesting that the effect of H₂ is to promote the growth of crystalline Si by preferentially etching amorphous Si and smaller nuclei rather than surface cleaning or roughening the SiO₂ substrate.

One approach to synthesis of large-grained polycrystalline films at a high deposition rate is the production of a low-density array of Si seed crystals at high H₂ dilution followed by growth at a high rate at low or no H₂ dilution. To test this idea, films were grown on SiO₂ at 60:1 H₂ dilution for 250 seconds, after which undiluted growth was allowed to proceed. As seen in Fig. 3, the resulting nucleation densities were higher than those previously observed for growth at 60:1 H₂ dilution, but lower than those observed for undiluted growth, suggesting that the high-dilution nucleation phase serves to suppress the formation of the numerous smaller nuclei that ordinarily form during undiluted growth.

CONCLUSIONS

Polycrystalline films have been grown on SiO₂ by hot-wire CVD at 0.17 nm/sec yielding a 40 nm grain size without the addition of H₂. The addition of 20 mT H₂ decreases the growth rate but produces films with grains of 85 nm in size. This increase in grain size is attributed to atomic H etching of amorphous Si and small crystalline nuclei, decreasing the nucleation density. The nucleation density increases sublinearly with time at low coverage, implying a fast nucleation rate until a critical density is reached, after which grain growth begins. We also produce large-grained films at a high deposition rate by nucleating at high hydrogen dilution and, once the nucleation phase is complete, growing rapidly at low hydrogen dilution.

ACKNOWLEDGEMENTS

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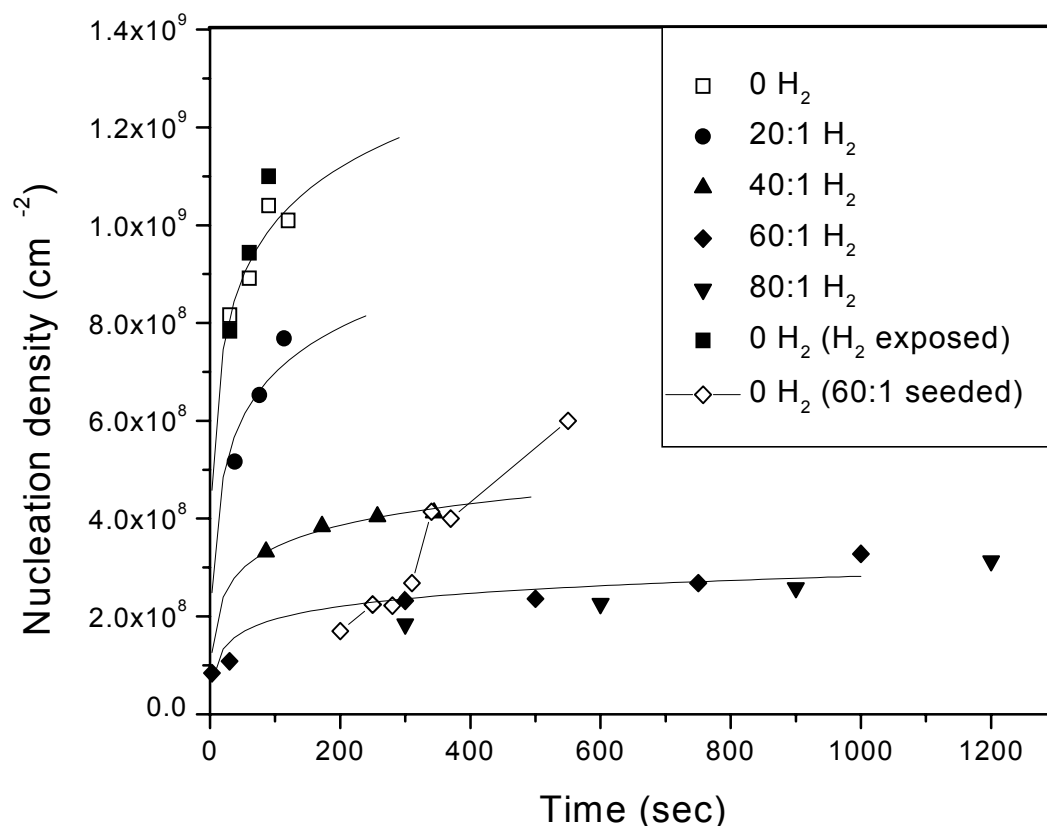


Figure 3. Nucleation density variation with time during low coverage poly-Si growth on SiO_2 , with data for concurrent H_2 dilution from 0-80 mTorr. Exposing the substrate to 60 mT H_2 before undiluted growth had no effect on the nucleation density. Undiluted growth on a low-density array of seed crystals grown at 60:1 H_2 dilution produced a lower nucleation density than undiluted growth on SiO_2 .

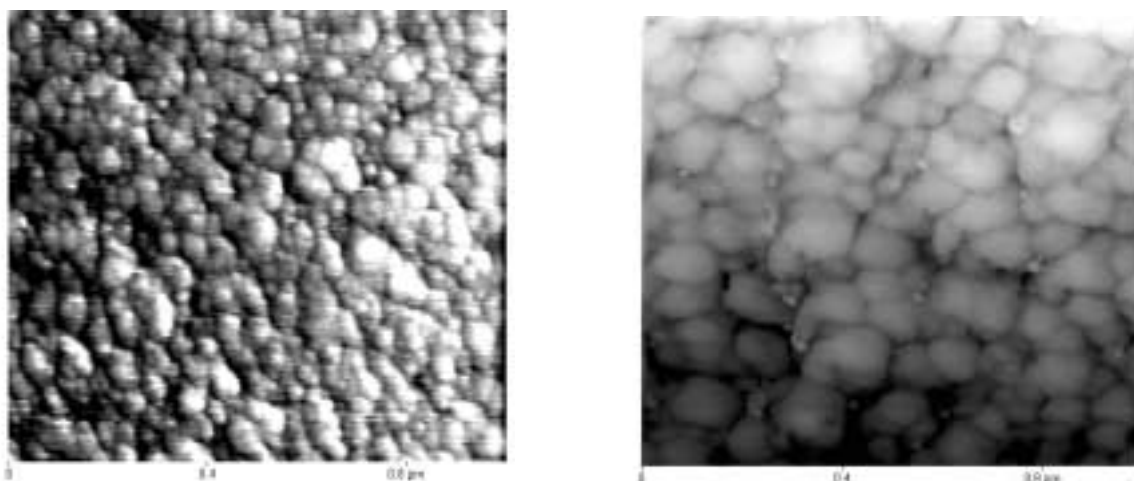


Figure 4. Post-coalescence $1\mu\text{m}^2$ AFM images of continuous poly-Si films. Left: Undiluted growth; grain size 40 nm. Right: 20:1 H_2 dilution; grain size 85 nm.

Ni-induced crystallization of poly-Si templates, and subsequent Si epitaxy

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The drive for high cell efficiency at lower cost in photovoltaics has stimulated research into thin-film silicon technology coupled with low-cost substrates, such as soda-lime or borosilicate glass. The low thermal stability ($<650^{\circ}\text{C}$) of these glasses has motivated low temperature approaches for making crystalline Si thin films. A promising process for application in low-cost thin-film crystalline silicon solar cells is selective nucleation and solid phase epitaxy (SNSPE) of Si with Ni nanoparticles as nucleation seeds. To make a polycrystalline layer thick enough to fabricate a solar cell, a sub-micron thick template layer is first made by SNSPE, and an active layer microns thick is epitaxially deposited on the template.

Metal induced crystallization of amorphous Si with Ni has been shown to occur below 600°C [1,2], making it compatible with the use of conventional low cost soda-lime glass substrates, and with growth rates much faster than other metal-induced crystallization with In and Al, or for unseeded growth. However, Ni has high diffusivity and high solubility in Si even at 600°C , which can result in Ni precipitates that act as shorts or carrier recombination centers. Previous studies of Ni content in Ni-induced crystallization of Si, using micro-Auger electron spectroscopy or x-ray photoelectron spectroscopy, did not detect any Ni in the crystallized region[1]. However, the x-ray fluorescence (XRF) microprobe at Lawrence Berkeley National Laboratory, which can detect Ni at levels below the detection limits of common analysis techniques, detected Ni in the crystallized region, but not in the amorphous regions. By determining where the Ni resides in the samples, as well as concentration, we can learn more about the crystallization process and whether using Ni-induced crystallization is feasible for photovoltaic applications.

In previous work[3], Ni was implanted into 75 nm thick a-Si with photolithographically defined crystallization seed regions. With vacuum annealing, seeded crystallization began at the Ni implanted islands (dose of $5 \times 10^{16} \text{ cm}^{-2}$) and continued by nickel mediated crystallization by fast propagation of branching needle-like crystalline structures, led by silicide particles[2], which

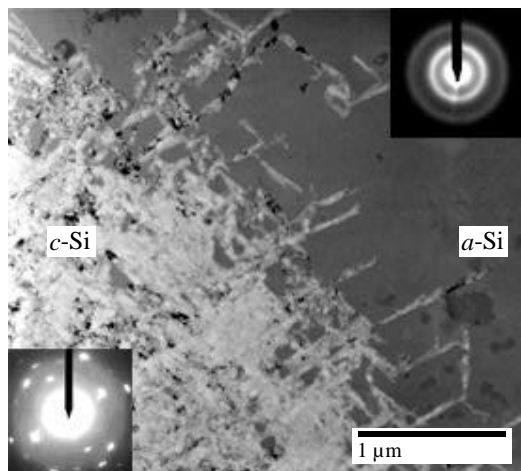


Figure 1. Bright field plan view TEM image of the growth front of a Ni implanted sample, with a dose of $5 \times 10^{15} \text{ cm}^{-2}$, annealed at 610°C for 65 min. The lighter region is the crystallized region, the darker area is the a-Si.

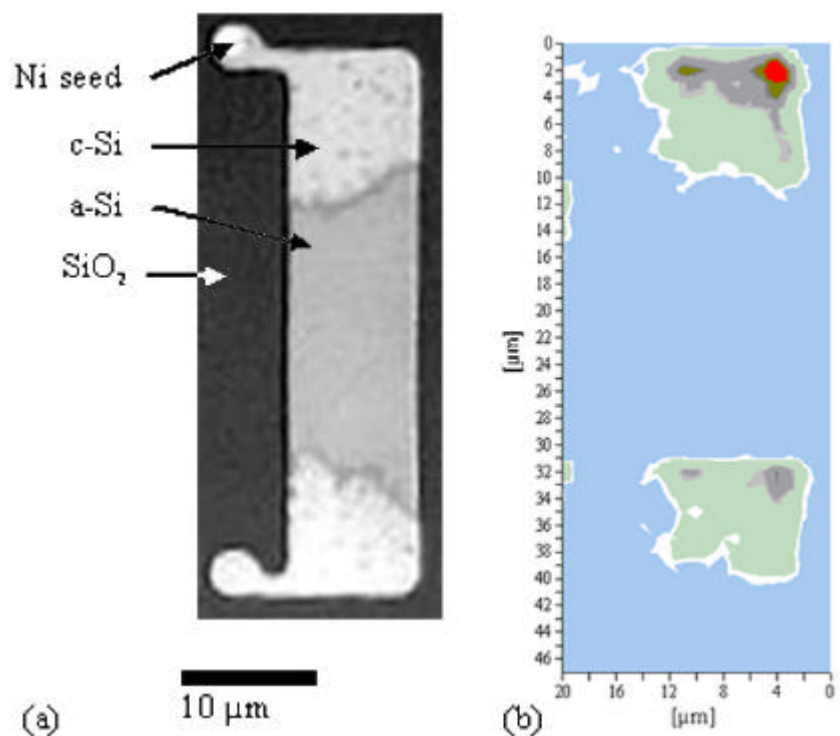


Figure 2. (a) Optical microscopy image and (b) x-ray fluorescence (XRF) microprobe scan of patterned Si. Clearly, the Ni signal from the XRF image corresponds with the crystalline regions in the optical image.

produced <110> textured substrates. A growth rate of 8 nm/s was attained for anneals at 610°C, compared to 1 nm/s for <100> oriented growth[4], or 0.02 nm/s for lateral polycrystalline growth[5]. Transmission electron microscopy analyses showed a large grain size but a high density of sub-grain boundary defects in the crystallized Si film (Figure 1). X-ray fluorescence microprobe analysis (Figure 2) showed that after some annealing, there was Ni in the crystallized Si above the detection limit of 1×10^{16} atoms cm^{-3} , but no detectable Ni in the a-Si regions. The Ni present in the crystallized portion is probably due to terminated crystallized trails with the nickel silicide on the edges. The average Ni concentration for fully crystallized samples is estimated to be 7×10^{18} cm^{-3} . A crystallized sample was used as a template for Si epitaxial deposition of a 1 μm thick Si film. Transmission electron microscopy analysis (Figure 3) showed a strong microstructural correlation between the substrate grain structure and the grain structure in the deposited layer, indicating local epitaxial growth. The final layer exhibited a large-grain morphology, with grain sizes larger than 4 μm .

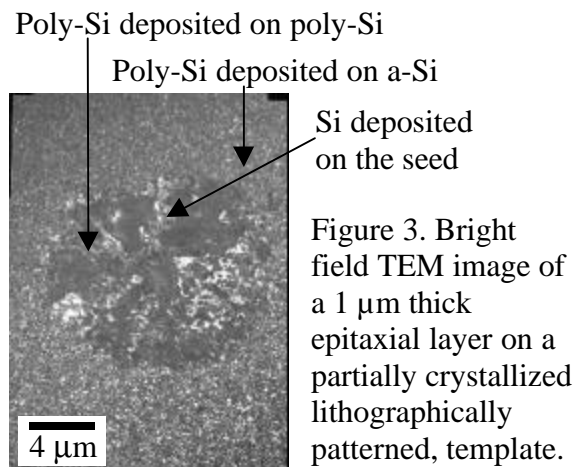


Figure 3. Bright field TEM image of a 1 μm thick epitaxial layer on a partially crystallized lithographically patterned, template.

To reduce processing costs associated with implantation and photolithography, a different Ni delivery method, with potential for non-vacuum processing, has been studied more recently. Ni nanoparticles with particle sizes under 200 nm, were mixed with isopropanol to a nanoparticle concentration of 20 mg/ml, forming a Ni "ink" that can be printed by an inkjet printer. After drying the ink, the 200 nm amorphous Si films were annealed at 600°C for 1 hour, producing grain sizes of ~30-40

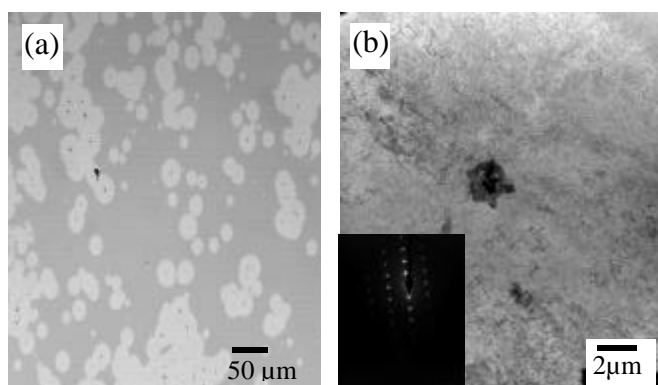


Figure 4. Images of polycrystalline Si crystallized by ink jet printing after 1 hr at 600°C. (a) Optical micrograph, with the crystallized Si visible as the lightest areas, and some Ni seeds visible as dark spots. (b) Bright field transmission electron micrograph of a Ni agglomerate in the center, surrounded by crystalline Si. Insert is a diffraction pattern of single Si grain.

μm (Figure 4). The growth rate was estimated to be over 9 nm/s at 600°C.

We will repeat the study of Ni concentration mapping in Si templates nucleated with Ni particles delivered by the Ni ink, as well as study diffusion of Ni into the epitaxial cap layer of Si. The 100 nm thick a-Si is cleaned with an RCA2 clean (5 H₂O:1 H₂O₂:1 NH₄OH) and then a HF dip, before applying the Ni ink, which is spun on, rather than printed. The samples are annealed at 600°C for 1-4 hours, and the Ni content analyzed with XRF. A microns thick epitaxial layer will be grown on the thin template layer. From the analyses, differences in Ni incorporation with different nucleation techniques and the degree of diffusion from the Ni-nucleated layer into the epitaxial layer will be studied. Ni concentration will be related to electrical measurements of minority carrier diffusion length and lifetime, using electron beam induced current and photoconductive decay.

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ENHANCED BULK POLYSILICON PRODUCTION USING SILICON TUBES

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Abstract

A novel technique using silicon tubes for the production of bulk polysilicon via chemical vapor deposition is presented. The polysilicon deposition rate increased as the total reactor pressure decreased and had a maximum rate of 0.66 $\mu\text{m}/\text{min}$ at 15 torr and 850°C. Our experimental studies with a model reactor indicate that the polysilicon growth inside of the silicon tube (15.3 g) exceeds that of the calculated polysilicon growth on silicon slim rods (4.3 g) over 55 hours of deposition time. These experimental studies have identified key criteria for the industrial prototype reactor being designed for bulk polysilicon growth. Initial cost estimations based on the proposed technology show that polysilicon can be produced at less than \$18/kg subject to variation in silane cost.

Key words: Bulk Polysilicon deposition, Chemical vapor deposition, Silicon tubes, Silane.

1. Introduction

Polycrystalline silicon or “polysilicon” forms the basic raw material that is used to grow single crystalline silicon, which is the most commonly used material for electronics, photovoltaics, and many other devices. An excellent review of the current world demand of polysilicon and its predicted growth is presented in [1]. One of the current methods to produce polysilicon is chemical vapor deposition (CVD) on resistively heated, thin silicon rods (about 6 mm diameter) in a bell jar using silane or tri-chlorosilane. This process is commonly known as the “Siemen’s process” [2]. If a metal rod other than silicon is used the process is referred to as the “Roger Heitz method” [3].

The diameter of the rod in the above processes (slim rod) increases with the deposition of silicon (Figure 1), but the process is very slow in the beginning because of the small surface area available for deposition. Varying levels of power must be supplied during the process to maintain the requisite reaction. Also, switching power from very high to low voltages is required during start-up and significant loss of energy to the environment make this process complex, less efficient and non-scalable. The upper limit of the silicon rod diameter thus produced is 12-15 cm. This is limit dictated by current reactor geometry and the magnitudes of currents flowing through the rods.

The only other commercial method that produces polysilicon beads is a fluidized bed reactor method [4]. This technique also suffers from several drawbacks, including: hydrogen inclusion, difficulty with melting the beads due to their large surface areas, low density of the solid (beads float), and production of much more undesirable silicon monoxide during the

growth process. Unfortunately, the method of polysilicon production has not changed since its early days except for better reactor design and computer control.

To substantially enhance the polysilicon production, we are investigating an innovative technique that will use silicon tubes instead of slim rods, in a CVD reactor for bulk polysilicon deposition (Figure 1). The tube(s) can be heated externally, thereby reducing the power consumption significantly and eliminating completely the requirement to pass current through silicon. The polysilicon yield on tubes can be substantially higher simply because of geometrical considerations (increase in surface area). There are no inherent up-scaling limitations on this process. In this work we present experimental results toward the development of this new polysilicon CVD technique.

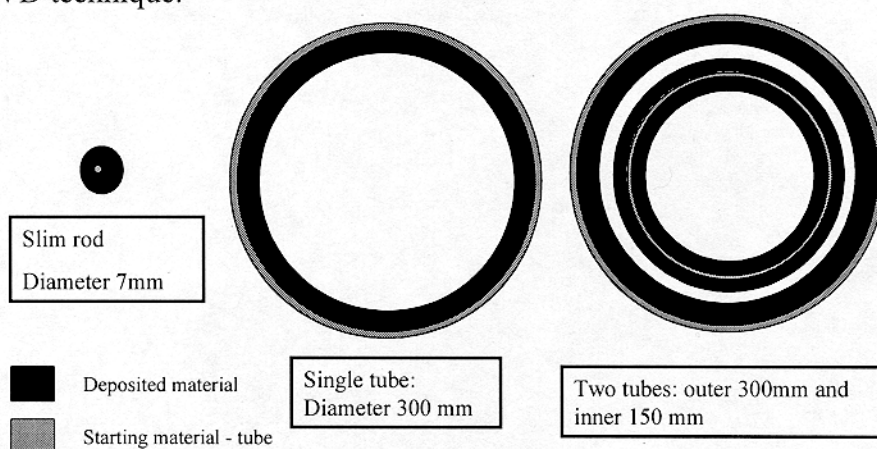


Figure 1. Schematic representation of polysilicon deposition on slim rod, single tube and two co-axially placed tubes.

2. Experimental Methods

The reagent gas was either a mixture of 1.46% silane in argon or 1.86% silane in hydrogen from Matheson Tri-Gas. Silicon wafers, and tubes used as substrate were cleaned with an $\text{HNO}_3\text{:HF}$ 8:1 solution for several seconds until the surfaces were shiny. The substrates were then rinsed with distilled water thoroughly.

Polysilicon was deposited using a custom-made hot wall CVD reactor with a resistively heated quartz tube of 3.4 cm inner diameter (see Figure 2). A gas inlet system with mass flow controllers allowed accurate delivery of known molar quantities of reagents. Following deposition, the SiH_4/H_2 mixture was stopped and Ar was started to prevent oxidation of surfaces at high temperature. The reactor cooled while maintaining Ar flow and the substrates were removed when the reactor reached ambient temperature. The silicon tubes (1.85cm inner diameter, 0.1 cm thick and 3.4 cm long) were placed in at the center of furnace by means of graphite tube (2.2 cm inner diameter, 0.5 cm thick and 4.5 cm long) holder as shown in the Figure 2 inset.

The deposition rate was determined by dividing the weight of the polysilicon deposited on the silicon wafer or the silicon tube by the accumulated deposition time (silicon density = 2.33 g/cm^3).

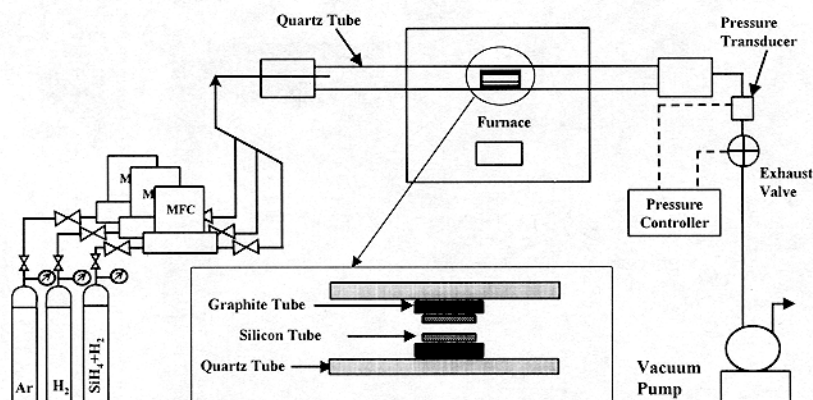


Figure 2. Schematic of polysilicon deposition reactor used for experimental modeling. The inset shows the cross-section of arrangement of the silicon tube inside the graphite tube.

3. Results and Discussion.

Figure 3 shows the variation of the deposition rate of polysilicon. Initial evaluation of deposition rates were studied on silicon wafers as a function of reactor pressure for various flows and reactor temperatures. Above 30 torr, the deposition rate is limited by the diffusion of the silane to the reaction surface. The higher pressures also result in significant powder formation. Below 30 torr, film growth rates are highest and there is negligible powder formation. The deposition rate at 15 torr pressure and 1000 sccm gas flow rate is comparable with the values reported in the literature, i.e. $0.6 \mu\text{m}/\text{min}$ [5]. The deposition rate is the lowest at 650°C with the SiH_4/Ar reagent mixture.

Figure 4 shows the weight of polysilicon deposition inside a silicon tube as a function of accumulated deposition time. The polysilicon growth inside the silicon tube increased with accumulated deposition time reaching a maximum of 15.3 g during 55 hours of total deposition time. This growth of the polysilicon is much higher than that on silicon slim rods (4.3 g, calculated assuming 0.6 cm diameter, 3.4 cm long silicon slim rod, 55 hours deposition time and $0.6 \mu\text{m}/\text{min}$ deposition rate).

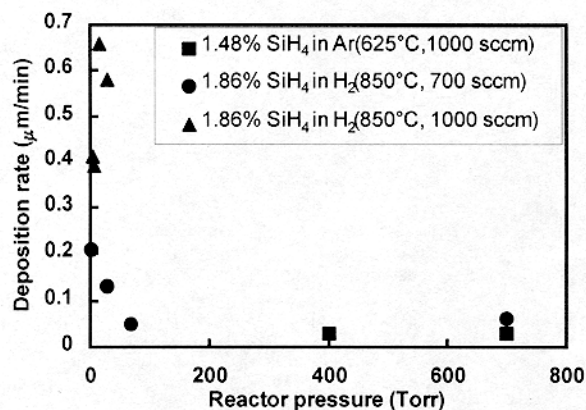


Figure 3. Variation of polysilicon deposition rate as function of total reactor pressure for various gas flows and furnace temperatures.

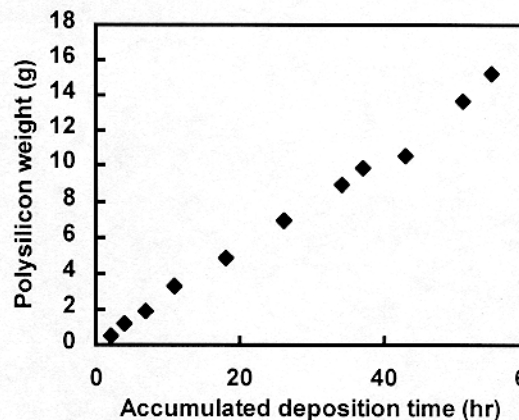


Figure 4. Polysilicon growth inside a silicon tube as a function of accumulated deposition time.

Figure 5 compares the estimated cost of polysilicon production for both the proposed and existing technologies based on silane cost of \$9/kg. The proposed technology produces polysilicon for < \$18/kg (compared to \$39/kg). This calculation includes capital cost, cost of raw materials and running cost. The throughput is estimated to be 56 metric tons/annum compared to the existing 38 metric tons/annum. This new technology produces virgin polysilicon, the purity of which depends on the quality of silane used.

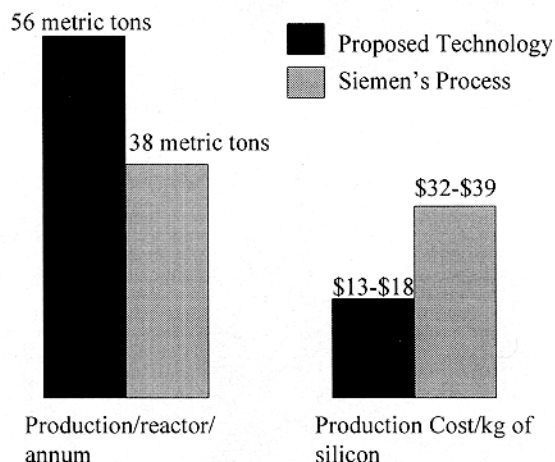


Figure 5. Comparison of production throughput per reactor and cost of production of proposed and existing technologies.

4. Conclusions

A novel technique for deposition of bulk polysilicon using silicon tubes is presented. The polysilicon deposition rate increased as the total reactor pressure decreased and had a maximum rate of 0.66 $\mu\text{m}/\text{min}$ at 15 torr and 850°C. The polysilicon growth inside a silicon tube increased with accumulated deposition time, reaching 15.3 g during 55 hours of deposition time. This is significantly greater than 4.3 g of polysilicon estimated to grow on a slim rod under the same conditions. The estimated cost of production of polysilicon, based on the prototype reactor design, shows that polysilicon can be produced at much lower cost than the existing technology.

Acknowledgements

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Transition-metal-hydrogen complexes in Si: Do structure-sensitive spectroscopies and DLTS study the same defects?

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In pioneering studies of the hydrogen passivation of deep-level defects in semiconductors, it was discovered that exposure of Si samples to a hydrogen-containing plasma can eliminate many of the levels associated with transition-metal impurities.[1] Until recently, little was known about the microscopic properties of the hydrogenated defects or the mechanism of passivation. Several recent studies provide new insight, but also show that the hydrogenated transition-metal impurities are more complicated than the early studies suggested.

New results come from several approaches.[2-5] In our work at Lehigh University, hydrogen has been introduced throughout bulk Si samples by annealing at high temperature (1250°C) in H₂ gas. In this way, a sufficient number of hydrogenated defects could be produced for study by structure-sensitive, spectroscopic methods like electron paramagnetic resonance (EPR) and vibrational spectroscopy. In these studies, structures were proposed for PtH, PtH₂, AuH, and AuH₂ complexes.[2,3] An additional surprising result was that these hydrogenated defects are electrically active!

A few other groups have used wet-chemical etching at room temperature to introduce hydrogen into thin surface layers of Si samples that also contained a transition-metal impurity.[4] In these studies, a number of new, electrically active transition-metal-hydrogen complexes were discovered and characterized by deep level transient spectroscopy (DLTS). An elegant analysis

of the shapes of the concentration depth profiles measured by DLTS has allowed the number of hydrogen atoms in the transition-metal-hydrogen complexes to be determined.

There would be considerable advantage if it were known with confidence that the structure-sensitive spectroscopies and electrical methods do indeed study the same transition-metal-hydrogen complexes. Unfortunately, typical samples used for DLTS experiments contain an insufficient number of defects for techniques like EPR or IR absorption. Conversely, samples prepared for structure-sensitive methods by high temperature annealing in H₂ gas and quenching are treated too roughly for DLTS experiments.

In this poster, experiments will be described in which IR absorption and DLTS were both used to study the same, or similarly prepared, samples. In one set of experiments, samples were prepared from a Si boule that had been doped with Pt during growth by the floating zone method. Hydrogen had been unintentionally introduced throughout the bulk of the crystal, presumably either from H₂ in the growth ambient or water from the growth-chamber walls. These bulk crystals have been ideal for studies by DLTS and IR absorption spectroscopy. The DLTS peaks and IR absorption lines assigned previously to PtH and PtH₂ were both seen in these floating zone Si:Pt samples, permitting the results of the two measurement techniques to be analysed together. In a second set of experiments, multiple-internal-reflection samples (inset in Fig. 1) were prepared so that the thin surface layers of hydrogenated defects that are produced in Si by etching could be studied by vibrational spectroscopy. Infrared absorption spectra measured by multiple internal reflection are shown in Fig. 1. The vibrational lines of small concentrations of PtH and PtH₂ defects ($\sim 10^{15} \text{ cm}^{-3}$) were detected in the thin surface layers ($\sim 5 \text{ }\mu\text{m}$) of Si:Pt that had been hydrogenated by etching. Our results support the conclusion that the structure-sensitive spectroscopies and DLTS study the same defect complexes.

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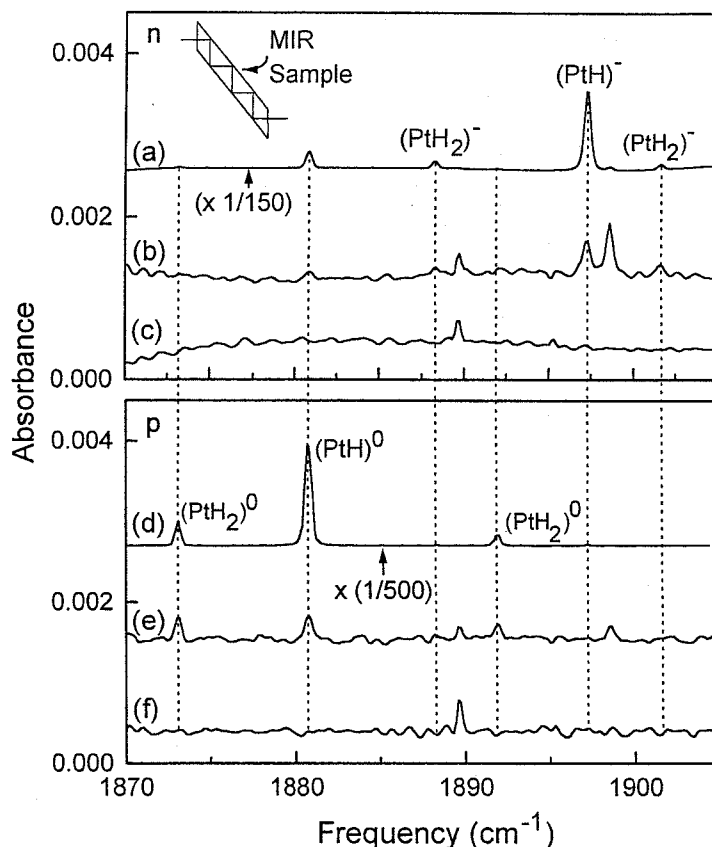


Figure 1. The inset shows the multiple internal reflection (MIR) geometry used to measure the infrared absorption spectra of n- and p-type Si:Pt samples. Spectra (a) and (d) show, for reference, the H-stretching lines previously assigned to PtH and PtH₂ complexes in bulk-hydrogenated, n- and p-type samples. Spectra (b) and (e) show the vibrational spectra of n- and p-type Si:Pt MIR samples that had been hydrogenated by a wet-chemical etch. These spectra show weak vibrational lines assigned previously to PtH and PtH₂ complexes. Spectra (c) and (f) show the vibrational spectra of the same MIR samples after they had been lapped and repolished to remove 50 μm from each surface. The vibrational lines produced by etching are absent, confirming that these vibrational lines arise from thin surface layers.

New synchrotron-radiation based technique to study localized defects in silicon: "EBIC" with X-ray excitation.

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Our recent analysis of the properties of iron and its complexes in silicon revealed that besides interstitial iron, iron-boron pairs, and iron-silicide precipitates, which were thought to be the major chemical states of iron in silicon, iron may form many other types of complexes and agglomerates. Complexes of iron with oxygen (iron oxides) or with oxygen and silicon (iron silicates) seem to be of particular importance for photovoltaics. This is because *mc-Si* wafers contain significant concentrations of oxygen along with trace concentrations of grown-in iron, and formation of complexes of these impurities are very likely. Unfortunately, very little is known about the chemistry, physics, and recombination properties of these compounds, partly because only few experimental techniques can locate them and identify the chemical structure of iron-oxygen-silicon complexes. These techniques are mostly X-ray analyses, which use synchrotron radiation to achieve sufficiently high sensitivity to analyze microdefects. One of the problems of application of X-ray microprobes to *mc-Si* is that one has first to locate the defects on the wafer. Usually this is achieved by either time-consuming scan of the wafer on the beamline, whereby the X-ray beam is moved slowly across the sample in hope that it will cross one of the agglomerates of interest, or by combining X-ray techniques with scanning electron microscopy (EBIC). Although EBIC enables one to easily find areas with low diffusion length, there remains a problem of how to move the sample to the beamline and focus the X-ray beam to precisely the same spot.

To simplify this task, we developed and demonstrated a new technique, X-ray Beam Induced Current (XBIC), which enables one to easily and quickly locate grain boundaries and electrically active defects without removing the sample from the beamline. This powerful in-situ technique can potentially be used to locate recombination active defects or p-n junctions, and may be used for elemental and chemical x-ray characterization of impurities in solar cells.

XBIC is essentially the same as EBIC except that the minority carriers are generated by monochromatic x-rays. As it is well known, EBIC technique is a very useful method for locating electrically active defects and junctions. In EBIC, the electron beam of the SEM is used to inject charge while in XBIC, the x-ray beam is used to generate minority carriers in a small region of the sample (numerous synchrotron x-ray beamlines have a spatial resolution in the .3 to 3 μm range, well within the range needed for beam induced current techniques). A synchrotron x-ray source provides an intense, tunable x-ray beam which is focused to approximately a 2 μm spot. The sample itself acts as a detector of electronic charge. What is then measured in EBIC and XBIC is the charge collection efficiency, which depends upon numerous spatially inhomogeneous factors including electrically active defects. Such defects reduce the charge collection efficiency. The detection of charge carriers requires some type of electric field either internally from a *p-n* junction or externally supplied by an applied voltage or both. The electron

beam or x-ray beam is scanned across the surface and the collected current is measured to form an image of electrically active defects.

However, there are some significant differences between EBIC and XBIC. In EBIC, the resolution of the image is primarily determined by the size of the electron cloud generated in the sample by the impinging electron beam, and can range from 1 to 10 μm depending upon the accelerating voltage of the electrons. For a narrow x-ray beam, similar resolutions would be expected. The depth distribution of the electron beam generated electrons is somewhat spherical while the x-ray generated depth distribution is determined by the exponential absorption profile of the x-rays. An interesting feature of EBIC or XBIC is that even very small defects, i.e. precipitates less than 80nm or decorated dislocations, can be easily imaged as micron sized features as long as the defects are highly electrically active.

At beamline 7.3.1.2 at the Advance Light Source, XBIC can be used in conjunction with microXPS to determine the chemical nature of defects. The x-rays at this beamline are generated by a bend magnet. An intense monochromatic x-ray beam with approximately $\approx 10^{10}$ photons/s focused to a $2\mu\text{m}$ spot in the soft x-ray range is delivered to the sample. In this work, we applied this technique to an edge-defined film-fed grown (EFG) polysilicon sample, slightly etched to remove any surface contamination. After an RCA clean, an aluminum diode of 3mm diameter and $\approx 300\text{nm}$ thick was evaporated on one side, and a 500nm Au diode was evaporated on the other side. The sample was inserted into beamline 7.3.1.2 using an automated sample transfer system. The sample holder makes an electrical contact when inserted with which to measure the collected current as a function of beam position and beam energy. No external voltage was applied, only the electric field from the aluminum Schottky diode was utilized to collect minority carriers.

Figure 1 shows an XBIC image taken using a photon energy of 1000eV and represents an

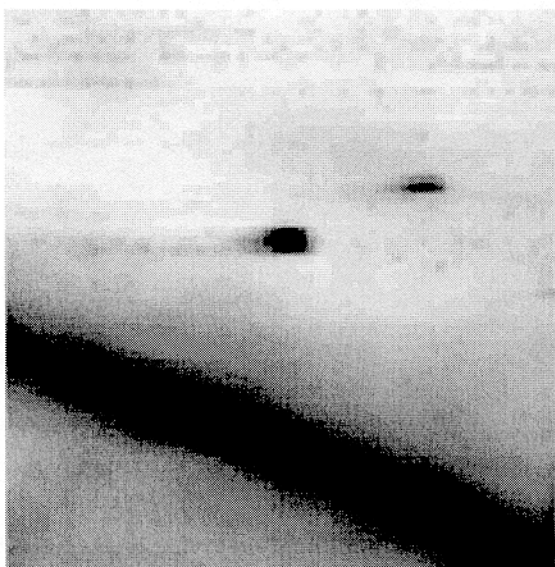


Fig. 1: XBIC image of a grain boundary and point defects. Xray energy of 1000eV has a penetration depth of approximately $2.2\mu\text{m}$ ($180 \times 180\mu\text{m}$)

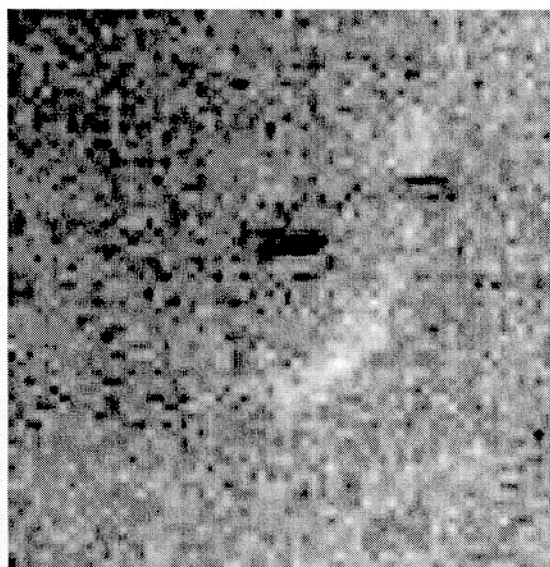


Fig. 2: Secondary electron image (any electrons from 2 to 20eV) of same area as in Fig. 1. The grain boundary is not observed in this image. The spots are observed, and are thus surface features.

area of $180 \times 180 \mu\text{m}$. A grain boundary can be clearly observed as the dark line. The dark line is approximately $30 \mu\text{m}$ wide. Since the grain boundary is physically much smaller, we can estimate that the electron generation volume is approximately on the order of $15 \mu\text{m}$. This wide generation volume is partially due to the fact that the photons enter the sample at a 60° angle rather than 90° . There are also two dark spots in the upper right hand corner. A secondary electron image of the same area, also taken using X-ray beam as a probe, is shown in Fig. 2 and the two spots are still observed. The grain boundary, however, is not observed in this image. Thus it can be concluded that the spots are a surface artifacts, either particulates or imperfections in the aluminum diode. At 1000 eV , the penetration depth of the x-rays at a 60° angle is approximately $2.3 \mu\text{m}$. The depth vs. photon energy for this configuration is shown in Figure 3.

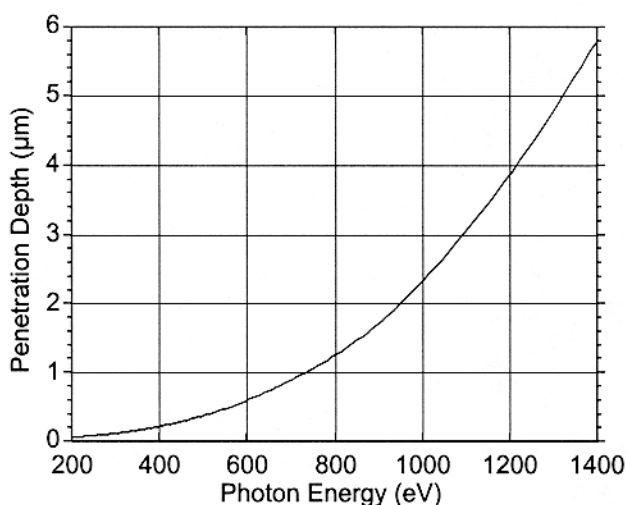


Fig. 3. Penetration depth as a function of photon energy with an incident angle of 60° .

The incoming photon energy can be adjusted, changing the penetration depth of the x-rays. In Figure 4, three images were made using different xray energies, 800, 950, and 1200 eV . As the photon energy increases, the x-ray penetration depth, the electron generation volume, and the total number of electrons generated, all increase. A by product is that the image contrast also increases as is observed in EBIC as the electron acceleration voltage is increased. One can see new features arise with increasing photon energy. This is a result of the increased penetration depth. Thus, the depth of an electrically active defect can be estimated by observing the onset of

contrasts as the photon energy is increased. In this case, there seems to be a precipitate at the grain boundary 3 to $4 \mu\text{m}$ below the surface. Again, the secondary electron image, shown for the 950 eV photon energy in Fig. 5, shows none of the features of the XBIC images proving that the XBIC features are not surface artifacts.

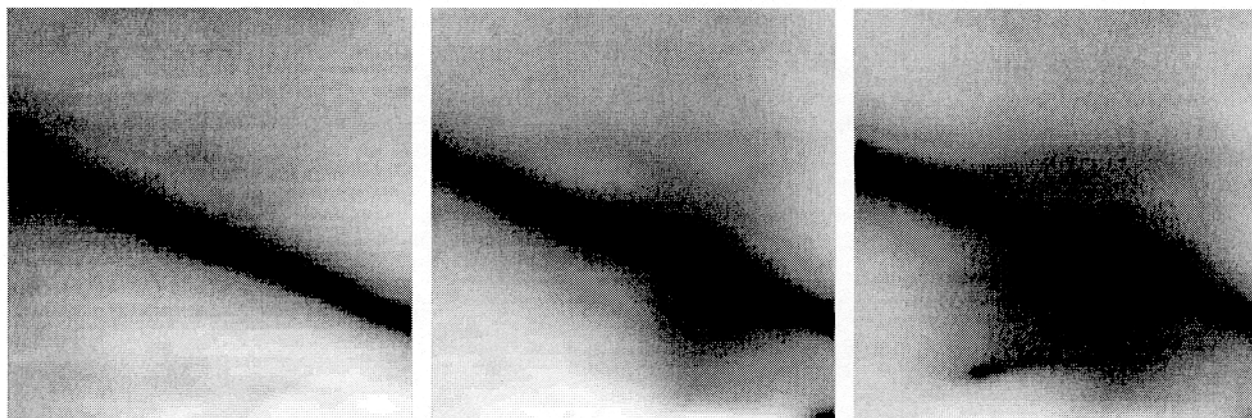


Figure 4: Series of images taken with various energies, 800, 950, and 1200 eV . These energies correspond to a penetration depth of 1.2, 2.0, and $3.8 \mu\text{m}$.

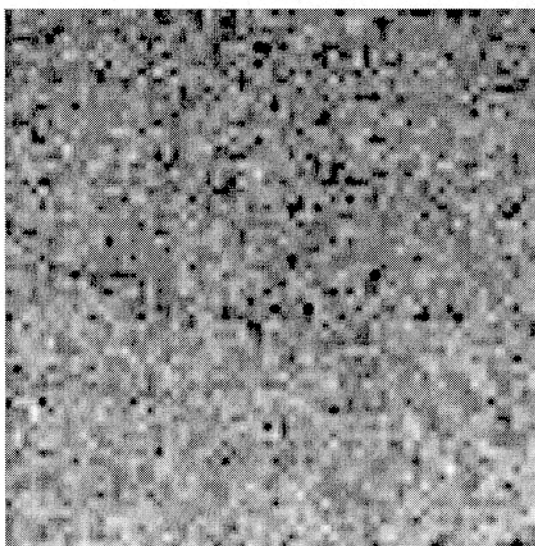


Fig. 5: Secondary electron image of same area at 950 eV. The grain boundary is not observed in this image.

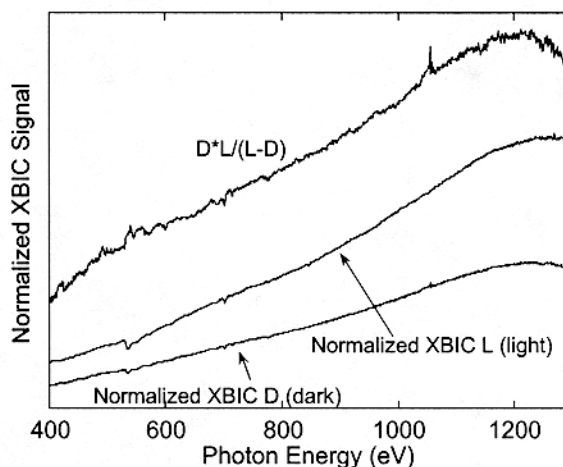


Fig. 6. The XBIC current normalized to the photon flux as a function of photon energy. The light and dark curves correspond to the light and dark regions labeled in Fig. 4. The light and dark curves were multiplied and then divided by the difference in order to obtain greater contrast.

Elemental information may even be obtained from the collected current. If the photon energy matches an absorption peak of an element in the x-ray probe volume, the resulting increase in the number of generated electrons would appear as an increase on collection efficiency, i.e. XBIC current. On the other hand, absorbing elements in the aluminum diode or at the aluminum-silicon interface would screen incoming x-rays, resulting in a drop of the observed XBIC current. In Figure 6, the XBIC current is shown as a function of photon energy for two spots in Fig. 4 labeled D (dark) and L (light). Since the incoming photon flux varies with photon energy, the XBIC current was normalized by the incident flux. The normalized XBIC current increases with photon energy due to increased generation of minority carriers at higher energies. The drop off in XBIC current at approximately 1200 eV occurs because the minority carriers are generated further from the Schottky diode depletion region and thus few minority carriers are collected despite the increase in the minority carrier generation at higher energies. There are two features on the normalized XBIC current curves. There is a dip (loss of flux) at approximately 534 eV on both the light and dark curves. This is likely absorption by oxygen in a thin Al_2O_3 film on the diode. This absorption is similar in both spots and does not show up in the difference curve, $D^*L/(L-D)$. On the other hand, a feature on the dark curve at approximately 1070 eV does show up as a on the difference curve. The feature is likely to be a phosphorous 1s absorption which has an energy double that observed. This absorption due to the second harmonic from the monochromator. Other phosphorous absorption peaks are less than 400 eV and are not observed. This brings up one of the difficulties of this method. If a defect exists at a given depth, only photon energies which penetrate to that depth or deeper, can be used to observe absorption.

In conclusion, we suggested a new method to facilitate the location of objects of interest in multicrystalline silicon for solar cell applications, and demonstrated it on the example of EFG material. On the next stages of the project, this technique will be applied for studies of recombination centers in solar cells.

Gas Phase and Surface Kinetic Processes in Hot-Wire Chemical Vapor Deposition

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ABSTRACT

Experiments and numerical simulations are being used to determine the parameters critical to high rate growth of high quality polycrystalline silicon via hot-wire chemical vapor deposition at silane partial pressures of 1-70 mTorr, and a wire temperature of 2000°C. In particular, the role of gas-phase chemistry in film growth is being explored via particle-based gas-phase simulation, mass spectrometry, and quantum chemistry computations. The Direct Simulation Monte Carlo method [1] was used, including gas-phase chemistry relevant for growth. Model predictions are in agreement with experimental measurements.

INTRODUCTION

Synthesis of large-grained polycrystalline silicon at low temperatures with high throughput is critical to enabling a future thin-film silicon photovoltaics technology. A promising approach for low temperature, high throughput film growth is hot-wire chemical vapor deposition (HWCVD). To this end, we are carrying out experiments and numerical simulations to explore the fundamental gas-phase and surface interactions of importance in HWCVD, and to optimize growth conditions for growth rate, crystal quality, and process uniformity. The simulations use the Direct Simulation Monte Carlo (DSMC) technique, a particle-based method that is the most appropriate simulation method in transitional pressure regimes where gas mean free paths are larger than wire dimensions, but smaller than wire-to-substrate distances. Critical to any simulation of the HWCVD environment is the inclusion of gas-phase chemistry, since the atomic silicon that leaves the wire is highly reactive and must be converted via gas-phase reactions to a less reactive precursor for high quality films (amorphous or polycrystalline) to result at low temperatures (under 400°C) [2]. Also important is the chemistry occurring at the wire and surface, and this is handled approximately by use of dissociative and reactive sticking probabilities, as described previously [2,3].

The present work aims to understand the relative roles in film growth of different gas-phase species in different growth regimes. Species often cited as leading to “high-quality film growth”, such as SiH₃, may only be effective in a certain range of film growth temperatures, for example. Another goal of this work is to characterize the effect of H₂ dilution on the gas-phase and film surface morphology. Hydrogen itself is involved in a number of the gas phase reactions of interest, suggesting that it may impact the distribution of potential growth species. In addition, recent results [4,5] suggest an increase in grain size and reduction in nucleation density with the addition of H₂. This is desirable for the particular photovoltaic applications in mind, since a lower grain boundary density will reduce the density of potential minority carrier trap sites.

MODEL DESCRIPTION

The DSMC technique is a direct, physical simulation technique whereby particles that each represent a large number of real molecules move, collide, react, and interact with surfaces in such a way as to produce collision and reaction rates that are statistically correct. The flow region is divided into a number of cells, each of which is sampled for particles, and the properties of those particles are averaged once steady state is reached to determine overall flow properties. A number of low density gas flow examples simulated by DSMC that have validated the technique are described in Bird [1]. Particularly for HWCVD, DSMC is preferable over continuum hydrodynamic techniques that are valid only at much higher pressures.

The primary reactions occurring at the wire are the decomposition of silicon hydride species and molecular hydrogen into atomic Si and H [6]. Silane is assumed to decompose with a probability of 0.7 [7], while H₂ dissociation is treated as an activated process, with an activation energy of 50 kcal/mol, resulting in a 0.14 reaction probability at 2000°C. Reactions at the substrate are treated as irreversible, with estimated reactive sticking probabilities [3]. The substrate is assumed to remain nearly fully hydrogenated during the deposition process [8]. An overall H balance is insured by adjusting the H₂ flux back into the gas for reactions involving

surface hydrogen exchanges. Etching of surface Si by H is also treated in the surface model, based on experimental measurements by Perrin [8].

HWCVD typically uses total pressures no greater than 300 mTorr, with SiH₄ partial pressures of 30 mTorr and under. As a result, bimolecular reactions are likely the only significant ones, with collision rates too low for stabilization of 3-body reactions. Table 1 lists the relevant bimolecular reactions used in the DSMC simulation [3].

Table 1. Bimolecular gas-phase reactions used in the DSMC simulation. The rate constant is given by: $k = A \exp(-E_a/RT)$. From Ref. [3].

Reaction	A (cm ³ /mole-s)	E _a (cal/mole)
(1) SiH ₄ + H \rightleftharpoons SiH ₃ + H ₂	7.8E14	4491
(2) SiH ₄ + SiH ₂ \rightleftharpoons H ₃ SiSiH + H ₂	1.3E13	0
(3) SiH ₂ + SiH ₂ \rightleftharpoons Si ₂ H ₂ + H ₂	6.5E14	0
(4) SiH + H ₂ \rightleftharpoons SiH ₂ + H	4.8E14	23640
(5) SiH + SiH ₄ \rightleftharpoons H ₃ SiSiH + H	1.6E14	0
(6) Si + H ₂ \rightleftharpoons SiH + H	1.5E15	31800
(7) Si + SiH ₄ \rightleftharpoons Si ₂ H ₂ + H ₂	4.0E14	0
(8) SiH ₃ + SiH ₃ \rightleftharpoons Si ₂ H ₂ + SiH ₄	6.3E13	0
(9) SiH ₃ + SiH ₃ \rightleftharpoons H ₂ + H ₃ SiSiH	7.0E12	0

RESULTS

An accurate treatment of energy transport in the HWCVD simulation is critical, since the rates of activated reactions depend exponentially on the local gas temperature. As a confirmation that the model is treating energy transport accurately, a temperature distribution was obtained using a two-dimensional DSMC simulation [9]. Figure 1 shows a temperature distribution under conditions of 128 mTorr total pressure of 1% SiH₄ in He. With an assumed wire temperature of 2273 K, located at the coordinates (2.5 cm, 2.5 cm), the gas near the wire is seen to be substantially colder, with a temperature of 381 K at a distance of 5 mm from the wire. Such results are expected for rarefied gas flows in which gas mean free paths are comparable or larger than the relevant length scale (the wire diameter).

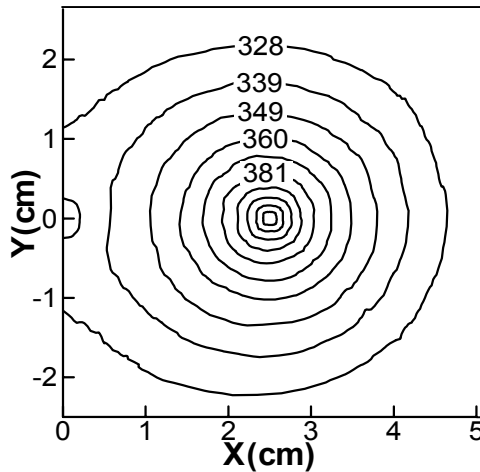


Figure 1. Gas temperature distribution in K for conditions of 128 mTorr total pressure (1% SiH₄ in He). The hot wire is located at (2.5, 2.5) cm, the gas inlet at (0, ± 0.25) cm, and the substrate at (5, ± 1.5) cm.

The DSMC simulation has also been used to address the question, what parameters can we adjust to increase the growth rate? One method explored was to increase the partial pressure of SiH₄. There is a limit to how high the SiH₄ pressure can be increased, however, due to potential radical-radical reactions [7] and gas-phase agglomeration of Si_xH_y fragments. In the case of dilute SiH₄ (1%) in He, our simulations predict that for approximately a factor of five increase in total pressure (128 to 590 mTorr), the SiH₄ depletion increases from 3.3% to 5.2%, providing a marginal improvement in growth rate. Another method of increasing the growth rate is to increase the utilization of SiH₄. Specifically, a decrease in the gas inlet-to-wire distance from 25 mm to 1 mm was found to increase SiH₄ depletion from 2.1% to 3.3% (at 128 mTorr of 1% SiH₄ in He). The overall small value of SiH₄ depletion predicted by the simulation is due in part to the small physical cross-section of the wire, dilution by He, and operating in a diffusive rather than convective flow regime.

Additional simulations of a pure SiH_4 ambient were run at pressures comparable to those of a study by Molenbroek *et al.* [10]. Figure 2 shows the results of these simulations, giving the SiH_4 depletion and Si_xH_y species flux at the substrate as a function of SiH_4 pressure. The species considered as the likely precursors to film growth were SiH_3 and Si_2H_2 . The former has recently been suggested [11] as leading to epitaxial growth on hydrogenated Si (100) at substrate temperatures as low as 195°C (dihydride coverage regime), and the latter has been suggested previously [2,3] to possibly play a role in film growth. Atomic silicon is also a potential growth species, but was less abundant under these conditions by several orders of magnitude; this species is highly reactive and is a potentially lower quality film growth precursor at temperatures below 400°C on hydrogenated Si (100). Atomic silicon has, however, been demonstrated to lead to epitaxy at temperatures in excess of 500°C , when complete H desorption occurs [12]. Silane depletion is seen to be substantially higher than in the case of He-diluted SiH_4 , and increasing with total SiH_4 pressure. The substrate flux of each of the two assumed growth species, SiH_3 and Si_2H_2 , is also seen to increase, with SiH_3 being the dominant contributor. Calculations of the growth rate corresponding to this SiH_3 flux compare favorably with the rate reported by Molenbroek *et al.* [10] under similar conditions, as illustrated in Table 2. Such agreement may indicate that the choice of species reactive sticking probability was appropriate. At substantially higher pressures, the flux (and

Table 2. Growth rate comparisons (L = wire-to-substrate distance)

Source	Conditions	Growth rate (nm/s)
Reference 10	$L=1.5\text{cm}$, 60mTorr SiH_4	10.3
DSMC simulation	$L=1.5\text{cm}$, 70mTorr SiH_4	9.6

thus growth rate) is expected to level off and then decrease as radical-radical reactions and agglomeration mechanisms become significant. These effects were not accounted for in this set of simulations, and thus predictions at higher pressures should be regarded as only approximate.

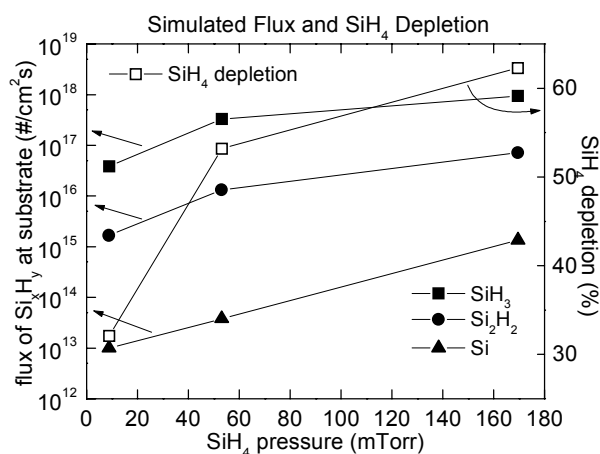


Figure 2. SiH_4 depletion and substrate flux of Si_xH_y species at different pressures of pure SiH_4 . The lines serve only as a guide to the eye.

In order to validate some of the predictions of the simulation and gain insight into the species involved in film growth, mass spectrometry experiments were conducted. Under low pressures (<100 mTorr total pressure of 1% SiH_4 in He) where gas-phase chemistry is not significant, species detected are those coming directly from the wire. Experiments in this pressure regime reveal primarily atomic silicon and hydrogen, in accord with observations by other groups [6]; atomic silicon is believed to be the primary growth species under these conditions. Subsequent experiments were conducted at significantly higher pressures (1000-2000 mTorr of 1% SiH_4 in He) at which gas-phase chemistry (Table 1; mainly, reactions 1 and 7) occurs. Specifically, the mass range 56-62 was explored because of the potential role of Si_2H_2 in film growth [2,3]. Figure 3 presents a mass spectrum acquired at 2000 mTorr and reveals predominately Si_2H , Si_2H_2 , and Si_2H_4 . The presence

of the latter two species is in accord with density functional theory calculations of the free energy profile for the reaction of Si with SiH_4 [13]; this profile is depicted in Figure 4. As the barrier for H_2 elimination from H_2SiSiH_2 is smaller than that for Si elimination, it is likely that Si_2H_2 will form. At these high pressures, however, the Si_2H_x signals were approximately 2-3 orders of magnitude smaller than those of SiH_x , and this is believed to be due to gas-phase agglomeration of these larger mass silicon species; in fact, powder was observed downstream in the chamber at these pressures. Subsequent experiments will probe the regime between 100-1000 mTorr in order to determine whether Si_2H_x species play any significant role in film growth.

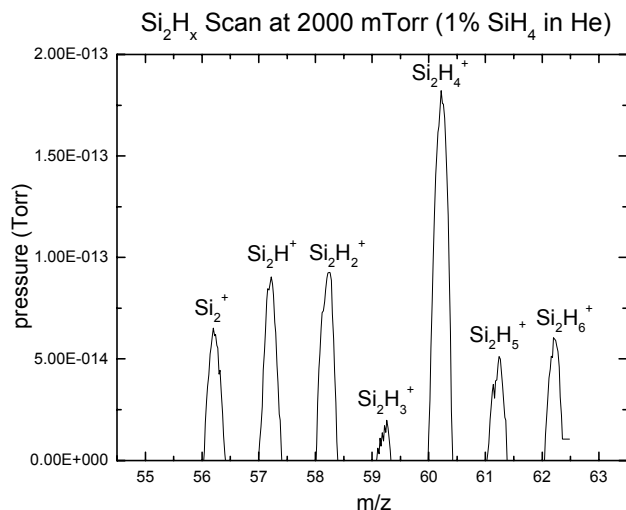


Figure 3. Mass spectrum of Si_2H_x species under conditions indicated.

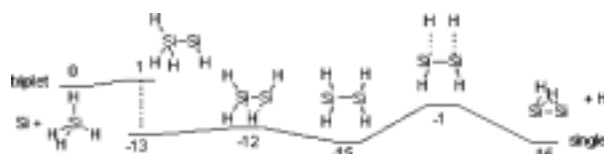


Figure 4. Free energy profile (kcal/mol) for the insertion, rearrangement, and H_2 elimination process that leads to Si_2H_2 [13].

CONCLUSIONS

Simulation of energy transport in HWCVD via the DSMC technique reveals a sharp temperature drop from the wire to the bulk gas. A method for increasing the growth rate appears to be an increase in SiH_4 partial pressure, although limits are imposed by the potential for gas-phase nucleation at extremely high pressures. Another method for increasing the growth rate is to increase the utilization of SiH_4 by decreasing the gas inlet-to-wire distance. The dominant growth species under pure SiH_4 conditions of 10-60 mTorr appears to be SiH_3 . A comparison between simulation and experimental growth rates reveals close agreement, with the choice of a reasonable reactive sticking probability. Finally, Si_2H_x species suspected of playing a role in film growth were predicted via quantum chemistry computations and detected experimentally.

ACKNOWLEDGEMENTS

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SUBSTRATE ROUGHNESS and DENSITY OF STATES OF POLY-Si FILMS DEPOSITED ON GLASS-CERAMICS

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I. Introduction

High-temperature-resistant inexpensive substrates that match the thermal expansion of silicon are required for the economical fabrication of polycrystalline silicon thin film solar cells. The ability to process the substrate at high temperature ($T > 700\text{ }^{\circ}\text{C}$) allows to achieve the high deposition rates of polysilicon necessary for economical mass production. However, most heat resistant glass substrates available at the moment soften at temperatures above $650\text{ }^{\circ}\text{C}$ [1]. High optical transparency of the substrates is also a key to fabricate “superstrate” cells, where the substrate serves as a cover glass. Fused silica is transparent and meets the temperature requirements but its thermal expansion coefficient is 1/5 of that of silicon, which introduces high tensile stresses in polysilicon films deposited at high temperature and makes them prone to cracking [2].

Glass-ceramics can be an attractive alternative to glasses used to fabricate the required substrates. These new materials withstand high temperatures and are currently used in consumer products such as range tops. They can be engineered to be transparent and match the thermal expansion of silicon [3].

Two aspects need to be considered to make glass-ceramics suitable to serve as substrates for thin film electronics. First, the out-migration of elements from the substrate to the silicon film must be prevented since many form deep level recombination centers for charge carriers. Second, the state of surface of the substrate needs to be carefully monitored since it is crucial for the performance of the thin film devices fabricated on this substrate. Surface roughness in particular influences the structure of the deposited polysilicon film and is known to affect device performance [4].

II. Glass-Ceramics

The glass-ceramics that are being investigated have recently been developed by Corning Incorporated [5]. The final microstructure of the glass-ceramic consists of 10-15 nm-sized spinel crystals dispersed uniformly in a siliceous glass matrix. The chemical composition of these materials lies within the system $\text{SiO}_2\text{-Al}_2\text{O}_3\text{-ZnO-MgO-TiO}_2\text{-ZrO}_2$. The glass-ceramic has a strain point over $900\text{ }^{\circ}\text{C}$ and thermal expansion similar to that of silicon.

To obtain a surface as similar as possible to that of conventional oxidized silicon and fused silica substrates, we polished glass-ceramic wafers using Chemical Mechanical Polishing (CMP). Figure 1a shows Atomic Force Microscope (AFM) images of CMP polished glass-ceramic wafer. The spinel crystals of about 10 nm in size dispersed throughout the siliceous glass matrix can be clearly seen in the AFM images. The distribution of the spinel crystals is confirmed by results of STEM analysis of this glass-ceramic [5].

Using CMP we reduced the surface roughness of the glass-ceramic to as low as 0.7 nm rms, however this value still remains higher than that of polished fused silica (0.3 nm rms) reflecting the different microstructure of the two substrates. The difference in hardness between the spinel crystals and the amorphous matrix leads to different local polishing rates that result in

the higher final roughness of glass-ceramics compared with the structurally homogeneous fused silica.

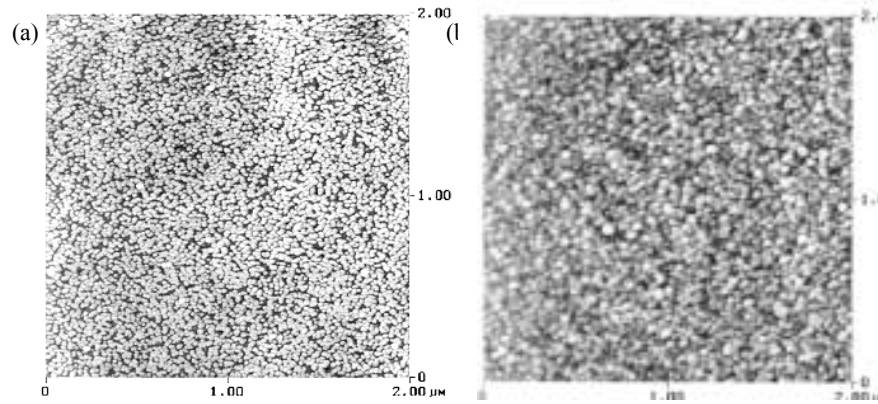


Figure 1. AFM images of the CMP polished uncoated (a) and barrier layer coated glass-ceramics (b).

III. Barrier layer

Some glass components, such as alkali atoms, are mobile at elevated temperatures and can migrate out of the substrate during high temperature processing. To prevent the out-diffusion of substrate components into the thin film electronics we developed an effective barrier layer.

A simple barrier layer consisting of 100 nm of SiN_x followed by 100 nm of SiO_2 was deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD). SIMS analysis performed on the samples annealed in nitrogen at 900 °C for 8 hours, indicates that 100 nm thick SiN_x is sufficient to stop out-diffusion. The top 100 nm thick SiO_2 layer serves as a low recombination surface for the thin polysilicon films [6].

The optical transparency of the barrier layer coated glass-ceramic was measured by Optical Transmission Spectroscopy (OT). Figure 2 shows the OT spectra of the uncoated and barrier layer coated 1 mm thick glass-ceramic wafers. Optical transparency was found to be over 95% in the visible range, a value that makes these substrates attractive as a ‘superstrate’ cover for solar cells.

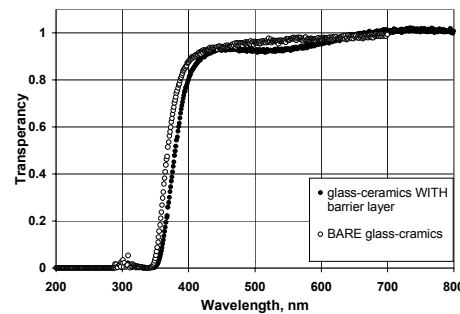


Figure 2. Optical transmission of uncoated and barrier layer coated 1 mm thick glass-ceramic wafers.

AFM analysis was performed to investigate the surface morphology of the glass-ceramic substrates. It was found that coating the substrate with the PECVD barrier layer resulted in a surface roughness of 1.2 nm rms (compared to 0.7 nm rms for the starting substrate). The AFM image (Fig. 1b) reveals features with average lateral size of 30 nm which were not detected on the surface of the CMP polished glass-ceramic wafers. These features are inherent in the structure of the barrier layer and their size (30 nm) does not depend on the surface condition of

the substrate. This phenomenon can be explained by considering the nature of the PECVD process. Due to the lack of thermal equilibrium in PECVD, the structure of the deposited film is determined by the process parameters rather than the surface conditions. However, both the intrinsic morphology of the barrier layer and the condition of the surface prior to its deposition contribute to the final roughness of the substrate.

Substrates coated with this barrier layer were used to fabricate thin film transistors to investigate the effect of the substrate on the electronic structure of the deposited polysilicon film.

IV. Density of states of polysilicon films

To evaluate various barrier layer and substrate systems, Thin Film Transistors (TFTs) were fabricated on thermally oxidized silicon (860 nm), polished fused silica, barrier layer coated fused silica and barrier layer coated glass-ceramic wafers. TFTs are majority carrier devices that permit us to quantitatively characterize the electronic structure of thin polysilicon films. A detailed description of the fabrication process can be found in [7,8]. TFTs were hydrogenated in an ECR plasma and electrically tested. Analysis of the temperature dependence of the TFT transfer characteristics was used to map out the density of states (DOS) of the polysilicon films [9].

The DOS plots shown in Figure 3 reveal the difference in the structure of the films deposited on different substrates. The films deposited on the very smooth surface of oxidized silicon exhibit the lowest DOS value ($\sim 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$). The films deposited on the barrier layer coated glass-ceramic and fused silica substrates are about an order of magnitude higher. To verify the hypothesis of the effect of surface conditions on the structure and DOS of the deposited films, we analyzed films deposited on uncoated and barrier layer coated fused silica substrates. Using identical substrates with different surface roughness due to the presence of the barrier layer made it possible to separate the effect of surface roughness from the

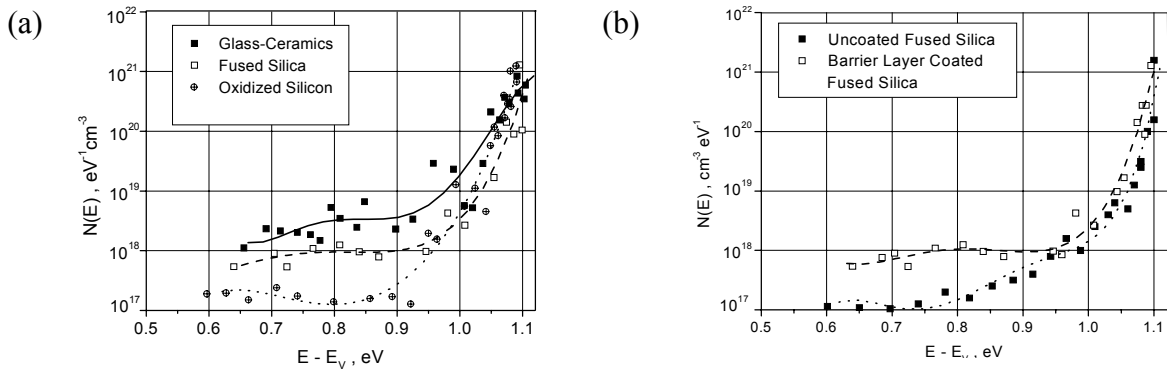


Figure 3. DOS of polysilicon films deposited on (a) oxidized silicon, barrier layer coated fused silica and glass-ceramic substrates and (b) on uncoated and barrier layer coated fused silica substrates.

effect of impurity out-diffusion from the substrate that also can increase the DOS. Since the fused silica wafers we used are of high quality and could not act as source of the impurities, the surface roughness was the only factor left to effect the DOS of the deposited films. Figure 3b shows that the DOS values of the film deposited on the smoother uncoated surface of fused silica are almost order of magnitude lower than that of the film on the barrier layer coated substrate.

TEM analysis of thin polysilicon films corroborates the results of our DOS measurements. Figures 4a and 4b show the TEM images of 100 nm polysilicon films fabricated on uncoated and barrier layer coated fused silica substrates. TEM revealed a fine (30 nm)

subgrain structure in the film deposited on the barrier coated substrate. The formation of this fine structure is traced to the surface of the barrier layer where similar features were found by AFM.

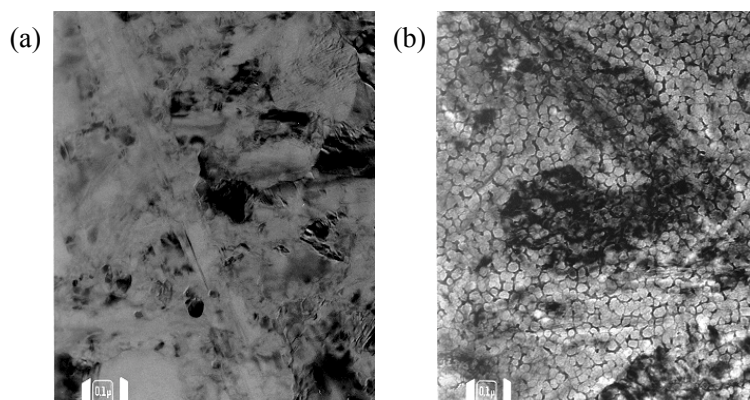


Figure 4. TEM images of polysilicon films fabricated on uncoated (a) and barrier layer coated (b) fused silica substrates. The films were deposited at 550 °C and then recrystallized at 900 °C.

V. Summary

We evaluated a combination of silicon nitride and silicon dioxide PECVD films as a barrier layer for novel high-temperature glass-ceramics. The developed barrier layer is highly optically transparent and very effective against the out-diffusion of mobile ions. The electronic structure of polysilicon films deposited onto these barrier layers was investigated and the surface roughness was found to be an important parameter determining the structure of the deposited polysilicon film. Further work will be conducted to develop smoother barrier layers.

Acknowledgements

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Radiative Properties of Materials of Interest to Thermophotovoltaics

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Abstract

A spectral emissometer, operating in the wavelength range of 1 to 20 microns, and temperature range of 300 to 1300 K, has been utilized to measure the radiative properties of quartz, polycrystalline sapphire, and erbium oxide. The significance of this study in the light of its applications to thermophotovoltaics is discussed.

Introduction

A thermophotovoltaic (TPV) power generation system converts thermal radiation directly into electrical energy. The thermophotovoltaic devices that make up the TPV system are semiconductor devices that convert photon energy from a black body-radiating source into electricity [1]. Several advantages of a TPV system are easy coupling to any thermal source, such as combustion or solar, quiet, non-polluting and easy maintenance since it contains no moving parts [2]. TPV has many advantages over conventional power systems. Some of these advantages are modularity, portability, wide choice of fuels, silent operation, reduced air pollution, rapid startup and high energy density. TPV might be used for portable electric power, standby electric power, stand alone electric power generation, residential cogeneration and clean electric vehicles [3].

Unlike the bandgap of silicon solar cells that is tailored for a heat source of ~6000K, the bandgap corresponding to the sun's visible light, the temperature of the flame utilized in TPV generators is of the order of 1500-2500 K. Cells built from the ternary compounds (with bandgaps that can be tailored to be between 0.25 and 0.5 eV) provide a much more efficient and denser source of electric power from the low temperature (compared with the sun) radiation source. InGaAs cells operate on the low end of the temperature range with the long wavelength infrared energy, while GaSb cells use IR energy, which has higher temperatures and shorter wavelengths. In order to achieve optimum usage of the emission spectrum, tandem cells are being proposed in which a GaSb cell is located behind an InGaAs cell so that both short and long wavelength IR energy generate useful power.

Since TPV systems utilize high-concentration power densities, the issues of radiator reliability and effective radiation coupling between the source of radiation and the semiconductor diode (PV cell) are extremely important [4]. The performance of a TPV converter is highly dependent on the selective optical properties of the emitter-filter-TPV cell back reflector configuration as well as the system geometry. Furthermore, there is a need to understand the sensitivity of the temperature gradient to the film and substrate

radiative properties. In addition, there are many materials, which have the potential for applications in TPV and their optical properties are unknown especially at high temperatures. Fig.1 shows a TPV generator, which burns natural gas inside a silicon carbide tube, and the emitter tube that glows red-hot. The TPV cells receive infrared photons from the emitter.

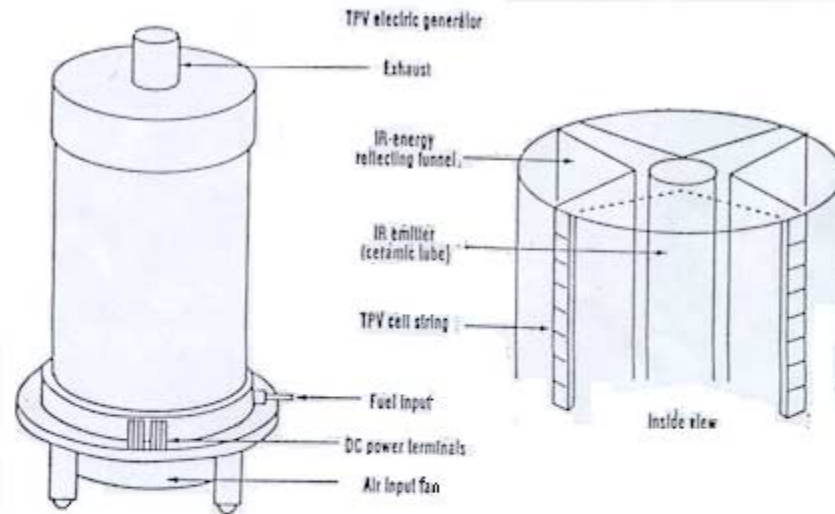


Fig. 1 Schematic of Electric Thermo-Photovoltaic (TPV) Generator

Experimental Details

The schematic of the spectral emissometer, utilized in this study, is presented in Fig. 1. The detailed operation of this instrument has been discussed earlier [5-8]. It consists of an hemi-ellipsoidal mirror providing two foci, one for the exciting source in the form of a diffuse radiating near-blackbody source and the other for the sample under investigation. A microprocessor controlled motorized chopper facilitates simultaneous measurement of sample spectral properties such as radiance, reflectance and transmittance. A carefully adjusted set of five mirrors provides the optical path for measurement of the optical properties. An oxy-acetylene/propane torch provides the source of heating of the samples. The spectral emissometer utilizes the Helmholtz reciprocity principle [9] as explained in a related study [10].

Experimental Approach

The spectral emissometer allows for simultaneous measurements of radiance R , reflectance ρ , transmittance τ and the temperature T of the sample at the measured point. The theoretical background and methodology is as follows [11]. A sample is placed at one of the foci of the hemispherical ellipsoidal mirror while the source, a blackbody at

900°C, is at the other foci. The chopper (in Fig. 2) permits the simultaneous acquisition of the radiative properties of interest including the sample temperature. A front-surface

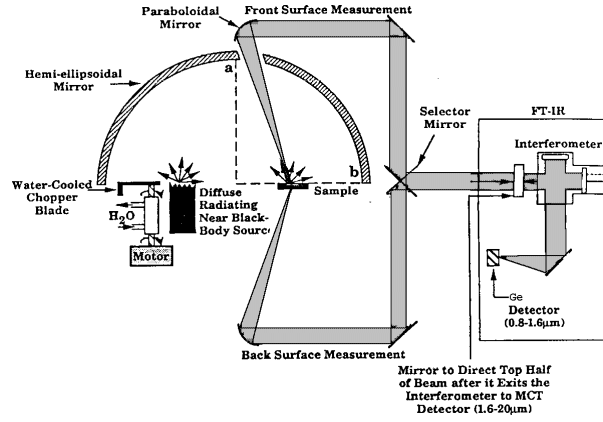


Fig 2. Schematic of bench top emissometer

sample measurement, with the chopper closed, yields the sample's directional spectral radiance:

$$R_v(T) = \epsilon_v(T)R_v^b(T) \quad (1)$$

Where, $\epsilon_v(T)$ is the emissivity of the sample at temperature T , and R_v^b is the theoretical Planck function at temperature T . The subscript v denotes the spectral frequency. When the chopper is open, the measured radiation M_0 will include that emitted by the sample and the blackbody source radiation reflected by the sample in spectral directional-hemispherical mode,

$$M_0 = R_v(T) + \rho_v(T)R_v^b(T_{bb}) \quad (2)$$

Where, T_{bb} is the constant blackbody source temperature, which is maintained at 900°C, and ρ_v is the spectral directional-hemispherical reflectivity. The difference in the two measurements is thus $\rho_v(T)R_v^b(T_{bb})$. The constant source radiation $R_v^b(T_{bb})$ is quantified by replacing the sample with a perfect reflector (a gold mirror, $\rho_{v\text{gold}} = 1.0$) and measuring the spectrum in the chopper open condition. Thus, the directional-hemispherical reflectance of the sample, $\rho_v(T)$, can be determined. For an opaque sample, the spectral emittance, $\epsilon_v = 1 - \rho_v$. By rearrangement of equation (1), $R_v^b(T) = R_v(T) / \epsilon_v(T)$, the surface temperature of the sample can be determined by direct integration over the whole spectral region,

$$\int R_v^b(T) dv = \sigma T^4 \quad (3)$$

The Stefan Boltzmann constant $\sigma = 5.67 \times 10^{-12} \text{ W} \cdot \text{cm}^{-2} \text{ K}^{-4}$. The sample temperature can be obtained to within $\pm 10^\circ\text{C}$. For non-opaque samples, the directional-hemispherical transmittance, τ_v , is measured by flipping the selector mirror and measuring the back

surface radiance and back surface radiance plus transmittance. The source radiation is quantified with the sample absent, and the analysis to determine τ_v follows that for ρ_v . The more extensive closure relationship, $\epsilon_v = 1 - \rho_v - \tau_v$, is then used to determine ϵ_v . The temperature of the samples can also be determined simultaneously by fitting the sample's radiance to the Plank's black body curves.

Results of Radiative Properties of Thermophotovoltaic Emitter Components

NJIT in collaboration with the US Army CECOM at Ft. Monmouth [12] has performed measurements of the hemispherical transmissivity, reflectivity and emissivity of some TPV materials as function of temperature using the state-of-the-art Spectral Emissometer. These materials include - (a) quartz which will be used as filter elements that will be placed between an emitter and PV cells, (b) sapphire, translucent polycrystalline sapphire and alumina – these are potential candidates as substrates for selective emitters in TPV systems, and (c) erbium oxide bulk and film materials whose thickness has influence on emitter characteristics.

Pierce and Guazzoni have discussed the results of these measurements in detail [12]. Examples of the results obtained in this study are presented in Figs. 2 and 3. In Fig.3, the transmissivity, emissivity and reflectivity of a quartz sample are presented as function of temperature. As can be seen in this figure, quartz exhibits low reflectivity which is almost independent of temperature in the wavelength range of 1 to 5 μm . Up to 1.7 μm , its transmission is high followed by a subsequent decrease with a minimum occurring at 2.7 μm . This minimum is caused by the presence of OH radicals in quartz. Corresponding to this minimum in transmission is a maximum in emissivity of quartz at 2.7 μm . These

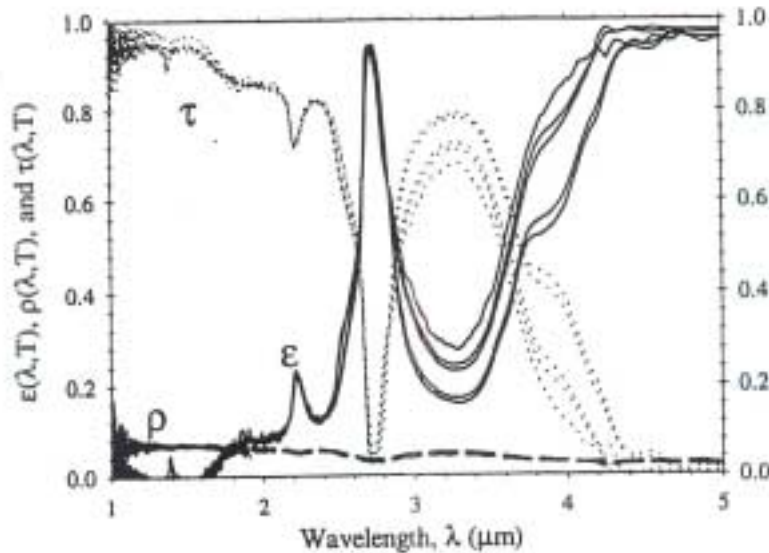


Fig. 3 Transmissivity, emissivity and reflectivity of quartz at temperatures of 180, 270, 550, 640 and 820 °C measured using the spectral emissometer [12].

measured data are useful in understanding the total radiation available from an emitter after being filtered through quartz.

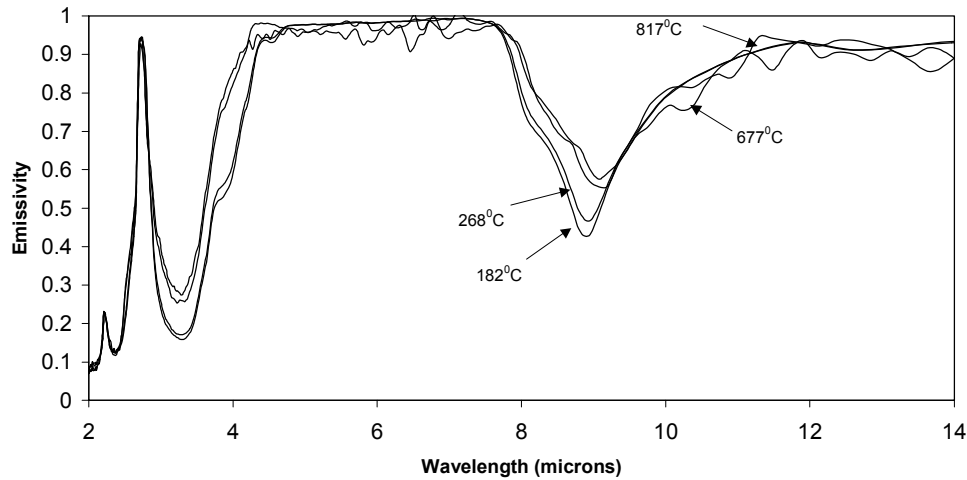


Fig. 4 Temperature dependent emissivity of quartz

In Fig.4, the temperature dependent emissivity of quartz at four specific temperatures, as measured using the spectral emissometer, are presented. As can be seen in this figure, quartz exhibits a sharp peak in emissivity at 2.7 μm followed by a broad peak in the 4.5 to 7.5 μm wavelength range. A dip in emissivity occurs at 9 μm with an increase and a saturation in the 12 to 14 μm .

Sapphire is a very widely used optical material. Its many applications include infrared windows, substrate material for infrared detector fabrication, silicon-on-sapphire, optical fibers etc. Sapphire is characterized by a very large transmission in the IR with a subsequent decrease at 6 μm . The measured emissivity of sapphire is presented in Fig. 5.

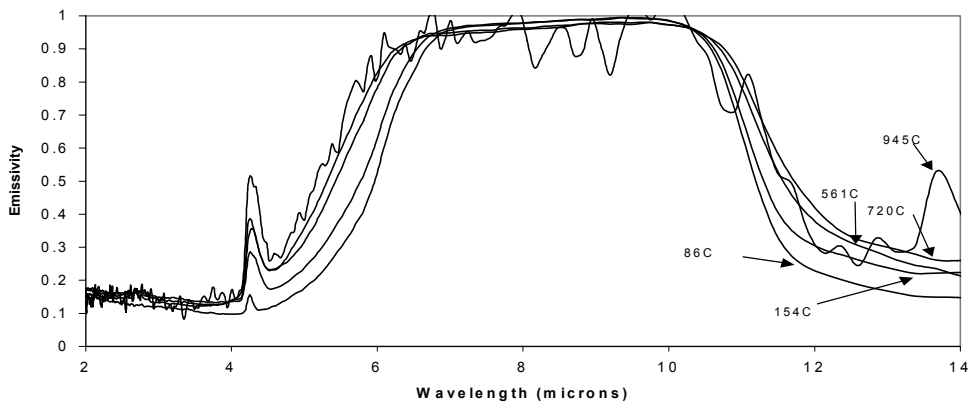


Fig.5 Temperature dependent emissivity of polycrystalline sapphire (lucalox)

As can be seen in Fig.5, lucalox exhibits a sharp peak in emissivity at 4.5 μm . In the wavelength range of 7 to 10 μm , its emissivity is maximum with a very broad peak.

High temperature optical properties play a critical role in determining the choice of materials for application as emitters in thermophotovoltaics. In Fig. 6, the emissivity of an erbium oxide pellet is compared with plasma spray deposited erbium oxide films of two different thicknesses. As can be seen in this figure, erbium oxide exhibits peaks in emissivity at wavelengths of 1.4, 1.53 and 1.64 μm . It also appears from this figure that the peak at 1.53 μm is approaching a saturation value faster than the other two peaks. These findings are useful in determining the optimal thickness required for an efficient erbium oxide based emitter for applications in TPV. The results of this study have been used to conceptually design an emitter using translucent polycrystalline sapphire as a substrate [12]. In addition, an attempt has also been made in this study to estimate useful rare earth film thickness by considering the molar absorptivity of the various rare earth ions in solution.

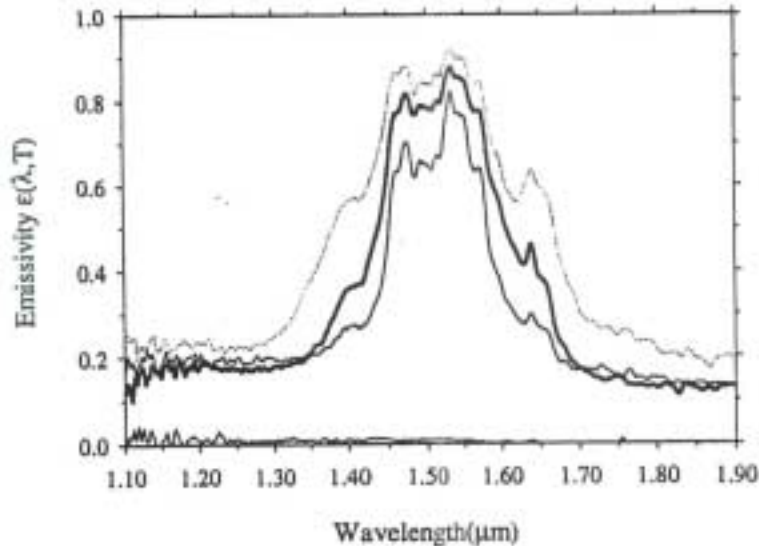


Fig.6 Emissivity of erbium oxide pellet compared with plasma spray deposited erbium.

Conclusions

Emissivity measurements of quartz, polycrystalline sapphire and erbium oxide have been presented in the above study. These studies have been performed, as function of temperature, using a spectral emissometer operating in the wavelength range of 1 to 20 μm . Application of this study to thermophotovoltaics has been discussed.

Acknowledgements

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PVSCAN 6000: A Tool for Analyzing Large-Area Substrates and Solar Cells

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Introduction:

Many photovoltaic (PV) companies are going to larger-area cells as an approach for expanding their production and lowering the PV energy cost. Attempt to increase the cell size is prompted by the fact that it is a simple way to increase the energy output without a corresponding increase in the cell processing cost. Unlike the fabrication of IC chips, the yield of solar cell is less dependent on the device area. As a result, it is more favorable and cost-effective for the PV industry to upgrade their production lines for larger area cell fabrication.

Larger cells do bring in a different set of problems. In general, larger cells exhibit stronger spatial variations in the photo-response—variations arising from local changes in its material quality, and due to nonuniformities induced by cell fabrication process steps. As a result, it is crucial to identify the nature of the cell nonuniformities and to mitigate their effects. PVSCAN has been designed to analyze solar cell material and device properties—to map their defect densities, near-junction and bulk photo-responses (both external and internal) and their reflectance behavior. In order to keep pace with the production trends, we have upgraded our PVSCAN to accommodate larger wafers and cells, and to perform measurements with higher speed.

PVSCAN 6000 system specification:

Our original PVSCAN 5000 was designed for 4-in x 4-in wafers and utilized scanning speeds below 1 inch per second. The upgraded system, PVSCAN 6000, can accommodate wafers and cells up to 8-in x 8-in in size. Other features are:

- Speed: 4-in/sec.
- Resolution: 0.002-in (highest resolution)
- Optical excitation laser wavelengths: 0.63 μm and 0.98 μm . These wavelengths are selected to separate near-junction properties from the bulk properties.

Other improvements:

The PVSCAN 6000 incorporates a variety of other hardware and software improvements, and wafer preparation methods.

Hardware improvements:

- Redesigned chassis to accommodate the larger x-y stage and a new vacuum chuck.
- Redesigned amplifier board to get higher gains.
- Upgraded motor controller from VF90 to VP9000 to drive larger motors.

- Changed 905 nm to 980 nm for deeper penetration into the bulk of the cell.
- Adjusted the beam splitter to get larger diffused-reflectance signals.

Software improvements:

- Changed commands/parameters to accommodate the new controller and data collection for faster scanning.
- Incorporated backlash compensation.
- Introduced a new display of distribution graph.
- Better color legend display.

Preparation of ribbon samples:

In the past, the defect mapping required that the wafer be chemically-mechanically polished prior to defect etching. However, we have streamlined the polishing procedure for wafers, but it is difficult to polish the ribbon flat. This is primarily because the ribbons have large variations in their thickness; the edges of the ribbons are typically thinner than the middle. Thus, polishing time for a ribbon can be very long. The longer polishing time is also caused by a high carbon content that increases the hardness of the ribbon material. Ribbon samples also have surfaces that exhibit striations. These rough surfaces can scatter light similar to that by dislocations, producing error in the measurement.

We have developed a procedure that obviates the need for chem-mech polishing of ribbon samples before defect etching. The ribbon samples are etched in a modified “Sopori etch” that delineates defects and smooths the roughness caused by striations.

Results:

Figure 1a is an LBIC map of a 3-in x 3-in section of a 6-in x 6-in cell taken with 0.63 μm laser excitation at a speed of 4 ips. Figure 1b is a corresponding map at 0.98 μm excitation. The distributions of the LBIC response are also shown in each figure. These two maps are able to determine that the variations are primarily related to nonuniform AR coating thickness.

Figures 3 and 4 show defect-maps and defect-distributions for Evergreen Solar and ASE Americas ribbons that were defect etched using the new procedure.

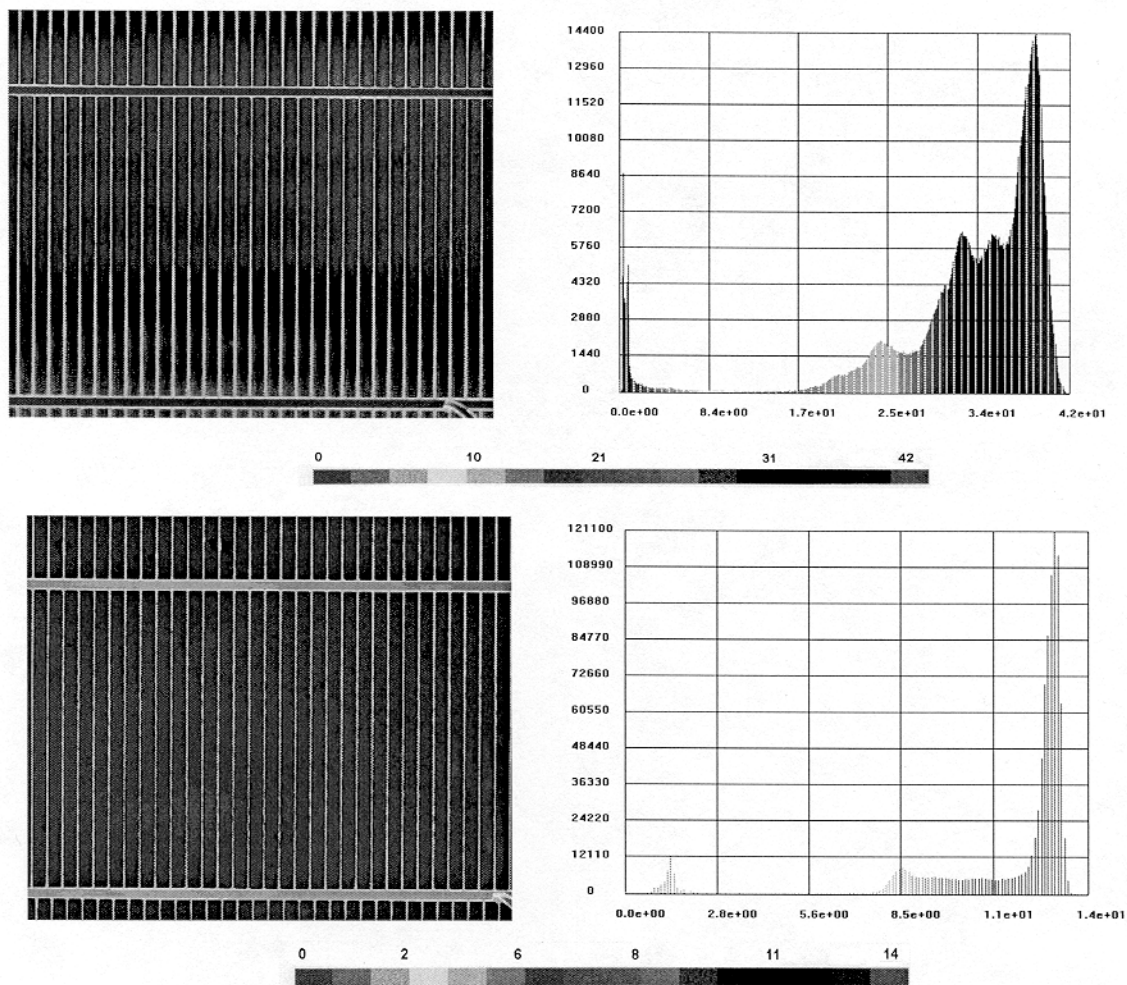


Figure 1. LBIC maps and the distributions of a 3-in x 3-in section of a 6-in x 6-in solar cell, taken at a scanning speed of 4 ips. The top and the bottom maps are taken at 0.63 μm and 0.98 μm laser excitations, respectively.

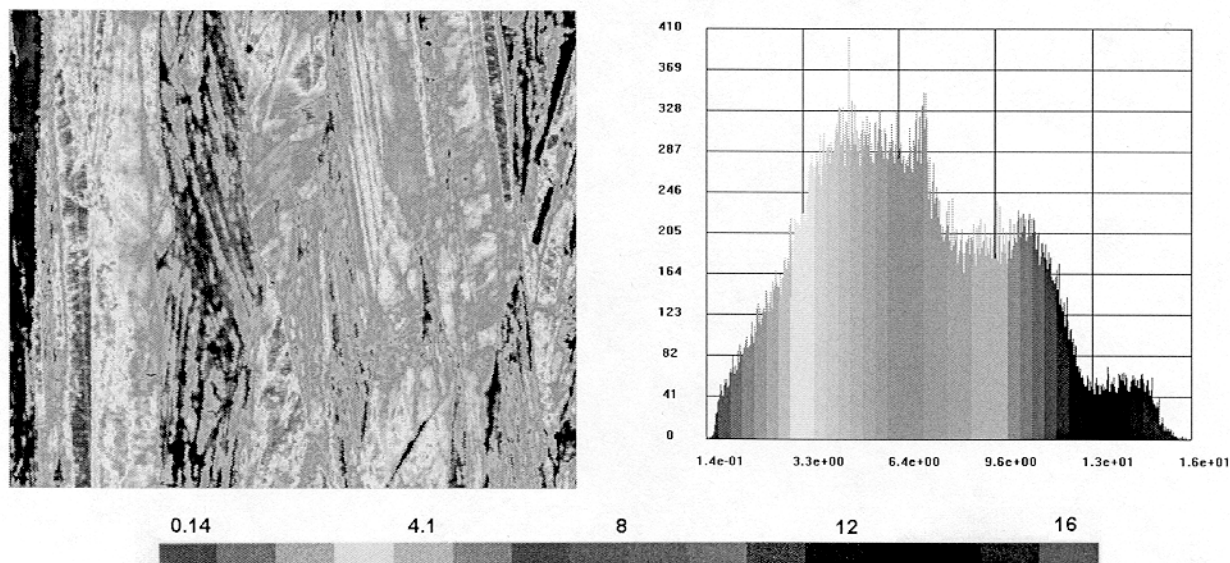


Figure 2. Defect map and distribution of a Evergreen Solar ribbon sample using new sample preparation. The color legend represents defect density in $1\text{E}6/\text{cm}^2$.

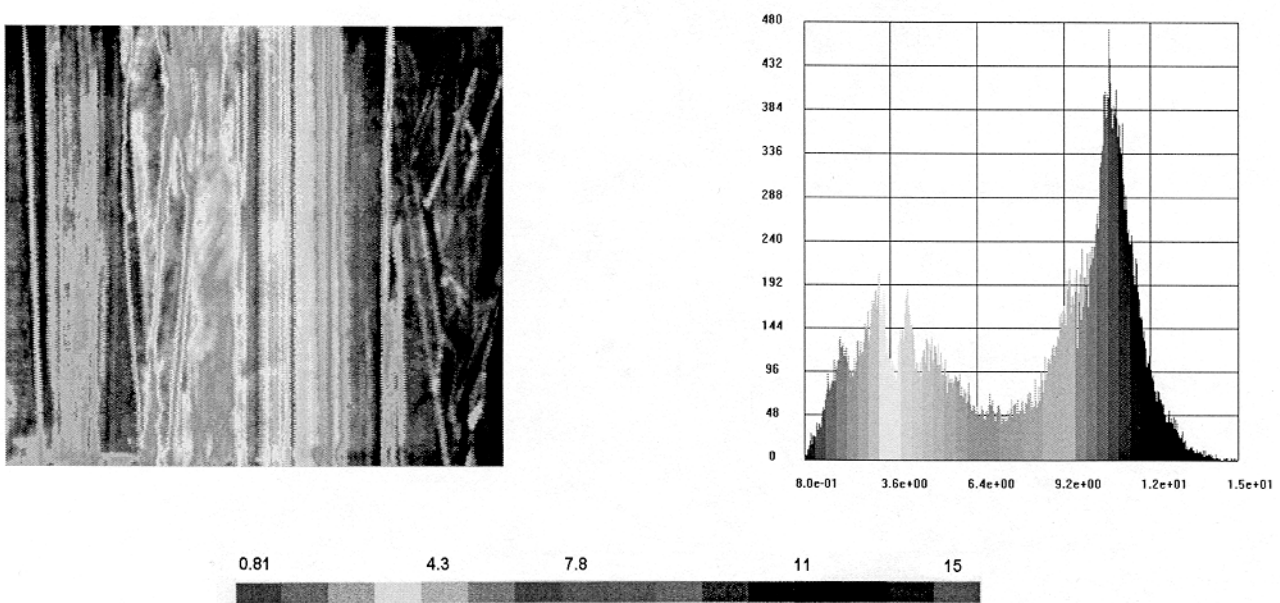


Figure 3. Defect map and distribution of an ASE Americas ribbon sample using new sample preparation. The color legend represents defect density in $10^6/\text{cm}^2$.

PRODUCTION OF SOLAR GRADE SILICON BY UPGRADING MG SILICON IN SIZES UP TO 140 KG

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ABSTRACT

It is intended to upgrade metallurgical grade (MG) silicon to produce solar grade (SoG) silicon meltstock. Thermodynamic calculations showed that it is necessary to remove boron (B) and phosphorus (P) to <1 ppma levels by refining; other impurities could be effectively reduced by directional solidification. Therefore, commercially available MG silicon, as received from the manufacturers, was melted in a modified Heat Exchanger Method (HEM) furnace, refined and directionally solidified. The refining approaches used were volatilization, slagging, and reactions to form impurity-enriched phases that can be removed from the silicon. Initial experiments using 1 kg MG silicon charge demonstrated that the B and P were reduced to 0.68 ppmw (1.77 ppma) and 13 ppmw (11.9 ppma), respectively. Based on this data, the charge size was scaled up to 140 kg and similar refining approaches yielded B and P concentrations of 4 and 11 ppmw respectively. Other impurities were reduced to significantly less than 1 ppmw levels. The most difficult element to remove from MG silicon is B and an effective B reduction process has been developed. Refining times were maintained as the charge size was scaled up. The simplicity of approach and economies of scale could result in production of SoG silicon.

SPUTTERED SILICON NITRIDE FOR MC-SI SOLAR CELLS

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ABSTRACT: The TwinMag sputtering technology is used to deposit hydrogenated amorphous silicon-nitride anti-reflection (AR) coatings on multi-crystalline (mc-Si) solar cells. Average cell efficiencies of 12.8% have been obtained on 12.5x12.5 cm² solar cells and the first 36-cell module with a sputtered nitride coating has an output power of 74 Wp. The experiments show that sputtered nitrides are excellent AR-coatings for solar cells. However, no bulk passivation has been observed yet. FTIR spectroscopy measurements showed that hydrogen is incorporated into the nitride as N-H bonds only and that the concentration of N-H bonds directly depends on the hydrogen content of the gas mixture.

1. Introduction

During the last decade it has become increasingly clear that hydrogenated amorphous silicon nitride (a-SiN_xH, abbreviated to SiN), deposited by means of Plasma Enhanced Chemical Vapour Deposition (PECVD), is a very promising candidate to act as a passivating anti-reflection coating (ARC) which increases the efficiency of mc-Si cells by more than 1% on an absolute scale [1,2]. The origin of the passivation effect lies in the combination of the large hydrogen content of SiN (up to 20 % at.) and the firing-through process of the metallisation. During this process Si-H and N-H bonds break and hydrogen diffuses into the mc-Si material and passivates recombination sites.

Much effort has been devoted at both research institutes and PV-manufacturers to develop and implement this technology into commercial production lines. Currently, only a few manufacturers have implemented PECVD, in most cases only on small scale, whereas other manufacturers still rely on high volume processes like APCVD TiO₂. The reason behind this is the lack of commercially available high-throughput in-line PECVD equipment. To overcome this problem, several initiatives are underway to develop equipment with planar or linear plasma sources [3,4].

Another approach is to look for alternative technologies where the volumes required for the PV-industry have been reached already for quite some time in other applications. Magnetron sputtering has become a leading production process with applications in the field of low emissivity and solar control coatings on architectural glass, antireflection coatings and transparent conductive layers on TV-screens and flat panel displays. Multi-chamber in-line systems with a throughput up to 8 million m² of glass per

year are commercially available at this moment. For reference, 8 million m² of solar cells with an efficiency of 13% equals 1000 MWp, i.e. more than 4 times the current yearly world production of solar cells [10].

While magnetron sputtering of SiN is a known technique, the challenge is to sputter hydrogenated SiN films with the same (or better) passivating properties as PECVD SiN. Fundamental research has recently been performed on this topic by Vetter [5] who showed that surface passivation of mono-Si wafers can be obtained by magnetron sputtered hydrogenated Si-rich SiN. The passivating properties on mono-Si and mc-Si solar cells have been investigated by Preu *et al.* [6] as well. They also observed that high quality surface passivation can be obtained with sputtered nitrides. The largest efficiency enhancement of PECVD SiN, however, comes from bulk rather than surface passivation. Surprisingly, this question has not been addressed in the previously mentioned studies. In this paper we therefore address the issue whether bulk passivation with hydrogenated sputtered SiN can be achieved on mc-Si solar cells in an industrial process environment.

2. Experimental set-up

For the experiments the TwinMag sputter technology [7] has been used. In this technology the sputter source consists of two identical planar magnetrons which are mounted side by side in the deposition chamber. The two magnetrons are driven by an AC power at a medium frequency of 40 kHz. At any time in this configuration, one magnetron acts as cathode while the other acts as anode. Positive charge that accumulates on the cathode during the negative-polarity half-cycles is neutralised by

free electrons during the following positive-polarity half-cycles. In this way no charge is build up and arcing is prevented. With this sputter source it is possible to deposit highly insulating materials like SiO₂, TiO₂ and SiN in a stable process.

The experiments were performed in the Leybold A400 lab system, which is equipped with a TwinMag sputter source. For the reactive magnetron sputtering process boron doped mc-Si blocks were used as target, N₂ as the reactive gas specie and Ar or a mixture of Ar/H₂ with 10% H₂ was used as the sputtering gas. For the experiments several gas conditions were used, as displayed in Table 1. For condition C1-C5, C7 and C8 the samples were not pre-heated and reach a temperature of approx. 50 °C during the sputtering process. For C6, the samples were pre-heated to approx. 220 °C before the deposition took place. For C7, the matching filter was changed in order to change the ion-bombardment. For C8, a short glow discharge was applied to the wafers prior to deposition in order to remove native oxides. The effective power was held constant during the experiments at a value of 8 kW.

Table 1. Sputtering conditions for silicon nitride antireflection coatings. For Ar/H₂-flow 10% H₂ is added to Ar-flow.

	Ar (sccm)	Ar/H ₂ (sccm)	N ₂ (sccm)	P (Pa)	
C1	100	-	170	0.2	-
C2	-	430	270	0.6	-
C3	-	430	170	0.6	-
C4	-	100	170	0.2	-
C5	330	100	170	0.6	-
C6	-	100	170	0.2	Pre-heated
C7	-	100	170	0.2	Matching filter
C8	-	100	170	0.2	Glow- discharge

Two types of experiments were performed:

a) Silicon nitride was deposited using condition C1-C4 on saw-damage etched p-type mc-Si wafers (Baysix, 0.5-2 Ωcm, 12.5x12.5 cm²). After deposition the wafers were subjected to a heat treatment in an IR-heated belt-furnace. The selected temperature profile is normally used for the firing-through process of metallisation on APCVD TiO₂ coated solar cells. Before and after this heat-treatment, the peak response of the wafers was measured with the Quasi-steady-state (QSS) technique [8] to see whether lifetime improvement takes place due to hydrogen passivation of bulk defects. In order to increase the sensitivity of the experiment for passivation effects we deposited the nitride on both sides on

the mc-Si wafers for condition C2-C4. On these samples also reflection measurements were performed.

b) 7 groups of 10 mc-Si neighbouring wafers each were selected from an ingot and processed until the emitter diffusion. Then SiN was sputtered as ARC using condition C1, C2, C4-C8. As a reference, one group was coated with a PECVD SiN. After deposition all cells were finished to complete solar cells by applying a screen-printed front and backside metallisation according to the well-known firing-through scenario. Fourier Transform Infrared spectroscopy measurements were performed with a Perkin-Elmer FTIR 1720 in the range of 400-4000 cm⁻¹ on coated mono-Si samples in order to measure the bonding configuration of hydrogen in the a-SiN_x-H matrix.

3. Results and discussion

a) Experiment on p-type wafers

After the deposition of the coatings for condition C1-C4 all coatings had a transparent deep dark blue colour. For condition C1, the optical appearance of the sample did not change due to the heat treatment, while for the hydrogenated samples clear changes in the colour occurred.

Table 2. Summary of optical and electrical results on the samples deposited under condition C2-C4.

Sample	Peakresponse QSS (V)	λ _{min} (nm)	R@λ _{min} (%)
C2 #1	0.624/ 0.135	580/ 580	0.42/ 1.67
C2 #2	0.624/ 0.135	580/ 580	0.42/ 1.67
C2 #3	0.055/ 0.127	580/ 580	0.32/ 1.39
C3	0.176/ 0.064	600/ 590	0.40/ 2.95
C4	0.138/ 0.069	610/ 600	0.45/ 0.50

In Table 2 the QSS lifetime measurements and optical measurements are displayed for condition C2-C4. The table shows that for all conditions C2-C4 with the exception of sample C2#3 the QSS peak response decreases significantly due to the heat treatment indicating, that the lifetime of minority carriers decreases. It is interesting to note that sample C2#3 has a very low response prior to the heat treatment in comparison to the other samples, while the response increases due to the heat treatment. The decrease in electrical performance goes along with some dramatic changes in optical properties. Table 2 shows that as a result of the heat treatment, the minimum reflection (R@λ_{min}) increases from typically 0.4% to more than 1%, while the wavelength at minimum reflection (λ_{min}) essentially remains unchanged. The latter

implies that the thickness and refractive index of the layer does not change. Instead, the increase in R can be explained by the large amounts of "pin-holes" or blistering of the SiN layer. This results in local areas without SiN and hence the reflection increases. The observed change in reflectance clearly corresponds to the hydrogen content of the gas-mixture, which is minimum for C3 and maximum for C2. For sample C4 the blistering is almost absent. Therefore, the reflectance at λ_{\min} remains almost constant before and after the heat treatment.

On the origin of the pinholes/blistering we can only speculate at this moment. Experience, however, has learnt that there is a correlation between these effects and surface contamination. The interesting new observation is that these effects appear to be mediated by the presence of hydrogen. For coatings deposited without hydrogen added to the gas mixture, the pinholes are absent and the coatings are stable during the heat treatment whereas for coatings with hydrogen, the pinhole density is large and increases with the hydrogen content of the gas mixture. A possible explanation is that contamination sites serve as nucleation points where atomic hydrogen is formed due to clustering and thereby causing high-pressure gas bubbles. These bubbles create enough mechanical stress during the heat treatment to crack the nitride film. This effect is well known in amorphous silicon [9].

b) Experiment on 12.5x12.5 cells

In Table 3 the average cell-characteristics of the cells from the different groups are displayed. It can be concluded that there is no significant influence of the sputtering conditions on the cell-parameters. The only significant difference is the higher J_{sc} and V_{oc} for the PECVD silicon nitrides, leading to an average efficiency of 13.1%.

Table 3. Averaged IV-characteristics for sputtered SiN under different conditions and one group with PECVD SiN. Standard deviation in $J_{sc}=0.3 \text{ mA/cm}^2$, $V_{oc}=3 \text{ mV}$, $FF=0.5\%$ and $Eff=0.2\%$.

Condition	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF (%)	Eff (%)
C1	28.2	591	75.6	12.6
C2	28.3	593	75.9	12.7
C3	28.3	591	75.5	12.6
C4	28.5	593	76.0	12.8
C5	28.5	591	75.9	12.8
C6	28.2	590	75.8	12.6
C7	28.3	589	75.5	12.6
PECVD SiN	28.9	597	75.7	13.1

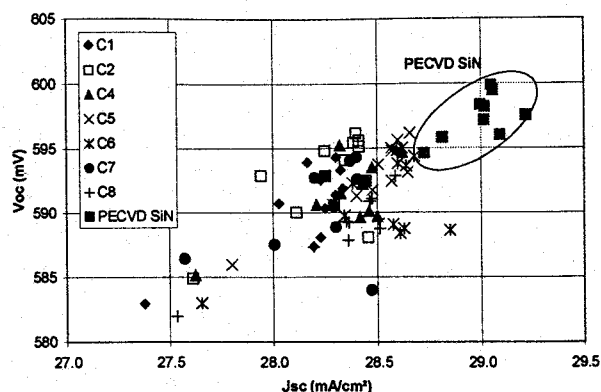


Figure 2. V_{oc} plotted against J_{sc} for the 7 different groups of sputtered silicon nitride coated samples and for the PECVD SiN coated samples.

In order to demonstrate the effect of bulk passivation and to show the influence of variation in base material quality, V_{oc} is plotted against J_{sc} in Figure 2. This figure clearly shows the absence of a significant influence of the sputtering conditions. The higher J_{sc} and V_{oc} of the PECVD group can be attributed to base material improvement due to H-passivation. Although no direct reference group with APCVD TiO₂ was included in this experiment, it is very likely that for the sputtered nitrides the effects of passivation are very small or even absent. The reason for this is, that the absolute values of V_{oc} , J_{sc} and efficiency are comparable to what is normally being obtained in production with APCVD TiO₂ on this type of cells [2]. It has to be noted that the relative improvement in efficiency of 3% for the PECVD group in comparison to the sputtered nitrides is lower than expected. Normally a relative efficiency improvement of 10-20% in comparison to APCVD TiO₂ can be obtained. This might be due to the fact that non-optimal settings were used during deposition.

In order to understand the absence of passivation for sputtered nitrides FTIR measurements were performed. Around 3000-3500 cm⁻¹ significant absorption was detected that can be attributed to N-H stretching bonds whereas between 2100-2200 cm⁻¹ no absorption was detected at all, indicating that there are no Si-H bonds present in the nitride. In Table 4 the measured peak area of the N-H absorption bonds in arbitrary units is tabulated for the various sputter conditions. The relative hydrogen content of the gas mixture is also calculated from Table 1. It can be seen that the peak area of the N-H absorption band directly correlates to the hydrogen content of the gas mixture.

Table 4. The measured peak-area of the N-H absorption bonds in arbitrary units for the different sputter conditions.

Process	H ₂ /(H ₂ +Ar+N ₂) (%)	Peak area (a.u.)
C1	0.0	0.0705
C2	6.1	0.9154
C4	3.7	0.4485
C5	1.7	0.3377
C6	3.7	0.4321
C7	3.7	0.4774
C8	3.7	0.4294

The absence of Si-H bonds is in contradiction with the work of Preu *et al.* [6] who also measured the hydrogen-bonding configuration for Twinmag sputtered SiN. A difference between both experiments is that Prue *et al.* used a hydrogen content of approximately 15% whereas in this experiment the largest content is more than a factor of 2 lower. The difference between these sputtered SiN and PECVD SiN coatings, is that the latter ones in general have both Si-H and N-H bonds and that the ratio between both bonds depends on the stoichiometry of the SiN [11]. For Si-rich nitrides hydrogen is pre-dominantly bonded to Si whereas for N-rich nitrides the predominant bonds are N-H. The absence of bulk passivation for the sputtered nitrides therefore may be related to the absence of Si-H bonds. However, it has to be concluded that the passivation effect of sputtered nitrides in relation to the bonding configuration of hydrogen is not understood and can be identified as a subject for future research.

Table 5. The IV-characteristics of mc-Si module with sputtered SiN ARC in comparison to an APCVD TiO₂ module (RSM75). The P_{max} for the sputtered nitride between brackets is the calculated value for a FF of 75%.

	Sputtered nitride	APCVD TiO ₂ (RSM75)
Voc (V)	21.7	21.6
Isc (A)	4.67	4.68
FF (%)	72.8	75.0
P _{max} (Wp)	73.7 [75.9]	75.7

Since all sputtered nitride cells had more or less the same IV-characteristics independent on the sputter conditions, the amount of cells enabled the possibility to produce the first 36-cell module. In Table 5 the IV-characteristics of the first sputtered nitride module and a 75 Wp APCVD TiO₂ module are listed. The results show that Voc and Isc of both modules are almost identical whereas the FF of the sputtered nitride module is slightly lower. Based on a 75%

FF the nitride module would have been identical to the APCVD TiO₂ module.

4. Conclusions

a-SiN_x:H AR-coatings have been sputtered on mc-Si solar cells using the TwinMag reactive magnetron sputtering technology. Average cell efficiencies of 12.8% have been obtained on 12.5x12.5 cm² solar cells. The first 36-cell module with a sputtered nitride AR-coating has been made with an output power of 74 Wp. It can be concluded that the sputtered SiN-layers are excellent AR-coatings for solar cells. Bulk passivation, however, has not yet been observed. More research is required in order to understand and improve the passivating properties of these nitrides.

Acknowledgements

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Enhanced Passivation for Multicrystalline Silicon Solar Cells by Co-sintering of PECVD-SiN_x and Aluminium

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ABSTRACT: This work takes a closer look at the interaction between bulk passivation by SiN_x (deposited by Plasma Enhanced Chemical Vapour Deposition) and the alloying process when forming an Al-BSF. Experiments on state-of-the-art multicrystalline silicon solar cells have shown an enhanced passivation effect if the creation of the alloy and the sintering of a silicon nitride layer (to free hydrogen from its bonds) happen simultaneously. All performed experiments show a similar effect as lifetime experiments done in [1]. The enhanced passivation is very beneficial for multicrystalline silicon, especially if the defect density is high, but it poses processing problems when considering thin (< 200µm) cells.

1. Introduction

Screen printed aluminium has found a widespread use for silicon solar cells, not only in laboratory but also in production lines. It is the easiest way to create an effective back surface field without unnecessarily complicating the process sequence. The Al-layer is normally printed over the whole back surface except for the strips of Ag/Al for soldering purposes. It is subsequently dried and fired (usually together with the front contact). During this firing at high temperature, the aluminium melts and forms an alloy with silicon according to their binary phase diagram. This typically results in a 5 µm deep highly doped p+ layer with an acceptor concentration around $5 \times 10^{18} \text{ cm}^{-3}$. The effective surface recombination velocity experienced by the base minority carriers can be quite low (< 1000 cm/s) due to the strong electric field present at this high/low (p/p+) junction. Because of the simplicity and the effectiveness of the process, Al-BSF has become the prime back surface passivation technique.

It is only in recent years that a suitable front surface and bulk passivation technique was found for industrial application. Nowadays the use of silicon nitride (SiN_x) as anti-reflection coating (ARC) and as a source of hydrogen for passivation purposes is generally accepted. While the deposition of nitride itself can result in a good surface passivation, an additional annealing step is needed to achieve a good bulk passivation, which is very important for multicrystalline and lower quality wafers. During the high temperature step, hydrogen is freed from its N-H and Si-H bonds in the nitride layer and can diffuse deep into the silicon to passivate defects [2]. In an industrial process sequence, this can be combined with the co-firing of the contacts. At this stage, the front contacts (Ag) are fired through the silicon nitride layer, which was deposited earlier, to make contact with the emitter. The Al-BSF is created at the same time. This passivation method has already proven its value many times [3].

A problem arises however when this process is transferred to thinner cells. A small disadvantage of aluminium is its low internal back surface reflection (around 70%). A more serious problem however is the bending of thin wafers due to the large difference in expansion coefficient between Al ($23.9 \times 10^{-6} \text{ K}^{-1}$) and Si ($7.6 \times 10^{-6} \text{ K}^{-1}$) [4]. For this reason, a lot of effort is put into finding a substitute for aluminium. The issue however is more complicated than just finding a replacement for the BSF. Earlier experiments at IMEC have indicated that the combined effect of firing the Al and SiN_x layer is larger than the two effects separately. This has also been shown in a recent publication by Rohatgi et al. [1].

2. Experimental evaluation

To investigate the possible interaction between silicon nitride passivation and the use of aluminium, the following experiment has been set-up: Multicrystalline Baysix wafers (size 10x10cm²) are processed into

solar cells according to different process sequences. All cells were identically saw damage etched followed by a POCl_3 -emitter diffusion. The rest of the process differed for the four groups that were made:

- Group 1: Standard process involving the co-firing of the PECVD-silicon nitride layer, the front contacts (through the silicon nitride) and the Al-layer. In this process, the creation of the BSF and the release of hydrogen happen simultaneously.
- Group 2: No BSF is created. The nitride is fired together with the front (Ag) and back contacts (Ag/Al grid: only a very small amount of Al is present in this paste in order to have a good contact with p-Si).
- Group 3: The Al is fired first resulting in a BSF. The eutectic layer is removed by hot HCl, followed by deposition of SiN_x , the printing of front (Ag) and back (Ag/Al grid) contacts and firing. The structure is exactly the same as for the first group. The only difference is that the firing of the nitride and the creation of the BSF do not happen simultaneously.
- Group 4: Similar to group 3, only the nitride is deposited on top of the front contacts (no annealing of the nitride layer)

Group 1 of the experiment is processed according to the standard screen printing process. In order to check the importance of Al as back contact, a second group was made using an Ag/Al grid instead of a full Al coverage. At first sight, a straightforward explanation for the rather large difference in cell results between the two groups (table 1) would be the influence of the Back Surface Field (BSF), which is present for group 1 but not for group 2. However, this explanation was doubtful since the wafer thickness is $330\text{ }\mu\text{m}$ and the diffusion length is smaller than that. Therefore the BSF should not have a very large effect. To test this assumption the third group was processed: In this case, the BSF was made first followed by removal of the Al-eutectic layer, deposition of the nitride layer, screen printed metallization of the contacts (Ag/Al grid for the back) and firing. The same results were obtained as for group 2 (no BSF) which indicates indeed that the BSF has no influence on the final cell results. It seems that the creation of the BSF together with the annealing of the nitride has a highly beneficial effect on the cell results. This is seen in the IQE-curves of figure 1 as an improvement in the long wavelength region and is indicative of an extended hydrogenation effect (since the BSF does not play a role) deep into the bulk of the cell. It has been proposed [1] that this enhanced effect is due to the creation of vacancies during the alloying process, which can facilitate the indiffusion of hydrogen into the bulk. Group 4 shows however that if the nitride layer is not fired at all, the results are still a lot lower. This indicates that the passivation effect from firing the nitride layer is present also when no Si-Al alloy is simultaneously created on the back surface (group 2). The effect can however be enhanced by the simultaneous creation of an alloy as can be seen from group 1.

Group	Process sequence	Jsc (mA/cm^2)	Voc (mV)
1	SiN (front) – Ag (front) – full Al (back) - firing	31.1	614
2	SiN (front) – Ag (front) – Ag/Al grid (back) – firing	29.8	604
3	Al (back) – firing – Al removal – SiN (front) – Ag (front) – Ag/Al grid (back) - firing	29.9	605
4	Al (back) – firing – Al removal – Ag (front) – Ag/Al grid (back) - firing - SiN (front)	27.8	589

Table 1: I-V results of different sequences involving SiN_x passivation and Al-BSF.

If the enhanced passivation effect is due to the creation of vacancies during the alloying then the effect should scale with the thickness of the p+ layer that is formed. To test this supposition, multicrystalline cells were made using a back contact paste with different Al-concentrations. All cells were fired at the same conditions so that the p+layer thickness (and the amount of vacancies) created in the process is also dependent on the amount of Al deposited on the wafer. The remainder of the process is identical for all wafers (saw damage removal, shallow POCl_3 -diffusion, plasma etching, SiN_x deposition, front and backside metallization, firing). The size of the cells was again 100 cm^2 , their starting thickness was $270\text{ }\mu\text{m}$. The results of these cells are shown in table 2. Figure 2 once more compares the IQE of the different cells.

Finally, table 2 also compares the extracted values for the Diffusion length (L) and the back surface recombination velocity using Basore's method [5].

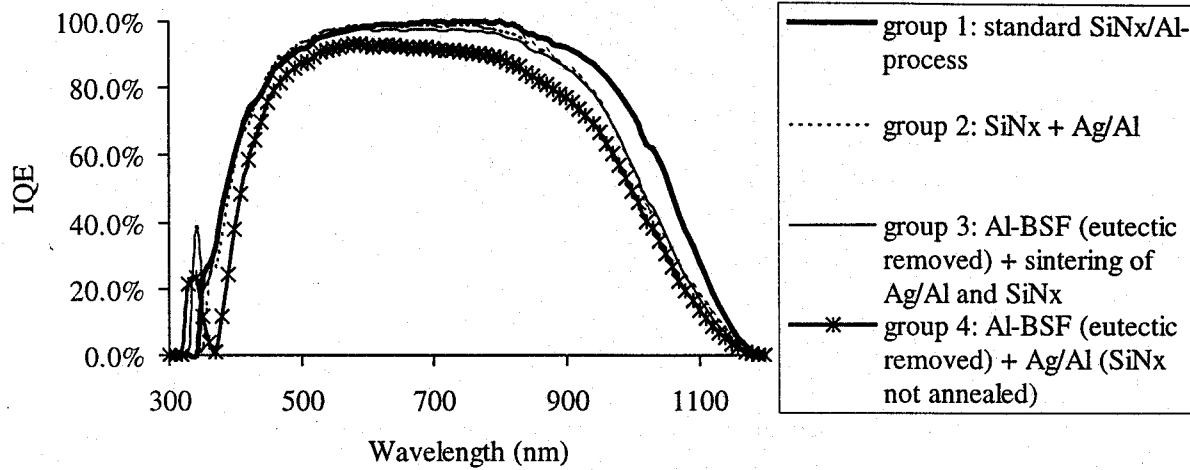


Figure 1: IQE measurements of different sequences involving SiN_x passivation and Al-BSF.

Back side paste	Jsc (mA/cm ²)	Voc (mV)	FF (%)	Eff. (%)	L (μm)	S (cm/s)
Al	32.1	618	76.8	15.2	261	1000
75% Al, 25% AgAl	31.6	614	76.4	14.8	224	1315
50% Al, 50% AgAl	31.4	612	76.5	14.7	172	2297
25% Al, 75% AgAl	30.5	606	76.1	14.1	115	34000
AgAl	30.3	603	74.2	13.6	(107)	-

Table 2: I-V results of cells with back contact paste (full coverage) with different Al-concentrations

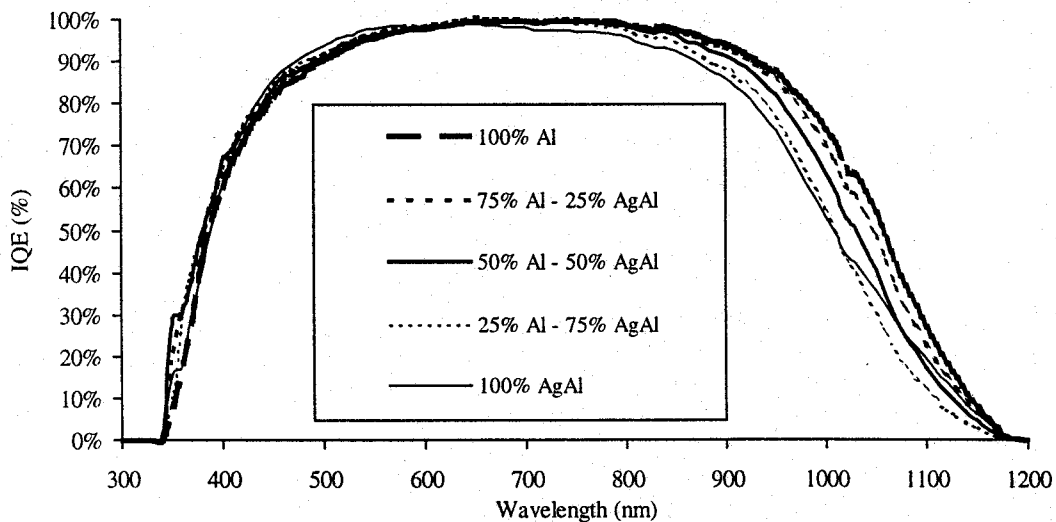


Figure 2: IQE measurements of cells with back contact paste with different Al-concentrations

The extracted values for the surface recombination velocity clearly show the effect of the BSF as expected for these thinner cells. More interesting however is the evolution of the diffusion length in the base, which also clearly scales with the Al-amount in the paste. This supports the hypothesis of an enhanced diffusion of hydrogen at high temperature if simultaneously an alloy is created. Remark the high IQE (figure 2) for the

cells with pure AgAl paste in the long wavelength region. This is believed to be due to a higher internal back surface reflection for this type of contact.

3. Short Discussion

The previous experiments indeed suggest that alloying Al with Si not only results in a BSF but also improves the bulk passivation of multicrystalline cells by enhancing the indiffusion of hydrogen. The vacancies that are created during the alloying process are very important for the creation of atomic hydrogen from the molecular hydrogen [6] that can be released by cross linking ($\text{Si-H} + \text{N-H} \rightarrow \text{Si-N} + \text{H}_2$) from the silicon nitride layer [7]. Furthermore a vacancy-hydrogen complex $\{\text{V-H}_x\}$ diffuses faster through the silicon wafer. This might explain the slightly higher IQE around wavelengths of 500 nm for the cells with a pure Ag/Al contact. In the last case a lot of hydrogen is available close to the front surface while this hydrogen can be distributed more uniformly over the wafer when a lot of vacancies are present. In the latter case this results in a higher IQE for the long wavelengths but a slightly lower one for the short wavelengths. The results from this work clearly indicate that, in order to benefit from the enhanced passivation effect, the creation of the alloy and the release of hydrogen from silicon nitride have to happen simultaneously. If they happen sequentially, no enhanced passivation is noticed. This could mean that the created vacancies during the alloying process are lost after cool-down and are not available afterwards.

All this makes finding a replacement for aluminium in order to avoid the bending of thin wafers not an easy task. Several ways to proceed are available: finding a replacement for Al in the alloying process, finding another way to create a large concentration of vacancies, optimising a Al-back contact pattern that diminishes the stress levels and bending problem, etc. This might become one of the most important tasks at the level of cell processing since the lower costs that are associated with thinner cells can only be benefited from if the cell efficiency can be maintained (or preferably increased).

4. Conclusion

Several experiments on multicrystalline silicon solar cells have proven that an interaction effect exists between bulk passivation by hydrogen from PECVD-SiN_x and the simultaneous formation of a Si-Al alloy on the back surface. This is a very beneficial side effect from using an Al-rear contact and is even much more important than the BSF-effect for thick multicrystalline silicon solar cells. Further investigations are planned to study this effect in more detail and to find an alternative for the case of thin cells where the bending of the wafer inhibits the use of a screenprinted Al rear contact.

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***Reduction of Light Induced Degradation in Czochralski Silicon Solar Cells by
Optimization of Cell Design Parameters***

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Abstract

Traditional Czochralski grown Si solar cells are known to suffer from light induced degradation (LID) which adversely affects the minority carrier lifetime. Recent methods that have been explored to reduce the effects of LID involve attempts to eliminate one of the constituents (Boron and Oxygen) that is responsible for the degradation via material growth or cell processing techniques. This paper shows that the effects of LID can also be reduced substantially by using thinner samples in conjunction with low back surface recombination velocity. A methodology is developed to determine the cell thickness that not only limits the LID but also maximizes the stabilized after LID. A combination of device modelling and experimental data is used to demonstrate that for a conventional Cz Si which undergoes a light induced lifetime degradation from 75 μ s to 20 μ s, optimum cell thickness is \sim 150 μ m for a BSRV on the order of 10^4 cm/s. This thickness reduces the light induced efficiency degradation from 0.75% for a 375 μ m thick sample to 0.24% absolute and gives the highest stabilized Cz cell efficiency.

Introduction

In an effort to maximize a stable efficiency on Czochralski grown silicon solar cells various techniques have been explored. Because light induced degradation, LID, has been directly related to B_i and O_i present in Cz wafers, one such method to obtain high stable efficiencies is to limit or eliminate the amount of B_i or O_i . This has resulted in some exciting results involving Ga doped Cz and B doped MCz (magnetic-Cz) with low O_i (< 1.3 ppma). By eliminating either B_i or O_i the defect responsible for LID is no longer able to form, thus avoiding any degradation [1-5]. Another method to reduce LID involves high temperature processing to precipitate the O_i which effectively reduces the trap formation. Even though this method has resulted in higher stable efficiencies on traditional high- O_i B-doped Cz Si solar cells with less than 8% relative degradation (1.5% absolute) [6], it requires specific high temperature treatments to maximize oxygen precipitation. Both of the above mentioned methods try to reduce the light induced trap density N_t . This paper shows an alternative method to reduce the harmful effects of lifetime degradation on cell efficiency by clever cell design involving cell thickness optimization which not only gives a smaller decrease in cell efficiency due to LID but also maintains a relatively high stable efficiency without any reduction in N_t . This methodology involves reducing the cell thickness and improving the BSRV to a point where the degraded diffusion length of the minority carrier is more than twice the thickness to maintain good electrical confinement of the carriers, and the optical losses are also not significant in the device. Reduced cell thickness not only decreases the LID but it also reduces the cost of solar cells. Cz silicon solar cells of varying thickness are fabricated and their performance is measured before and after 20 hours of LID.

Characterization and analysis is performed using modeling and experimental data, to demonstrate how to reduce the effect of LID by tailoring the cell design parameters.

Experimental

Boron doped Cz Si solar cells on 0.7 Ωcm material were processed using the dopant oxide solid source (DOSS) technique for various bulk thickness varying from 100 μm to 400 μm . The DOSS technique involves a simultaneous Phosphor and Boron diffusion from limited spin-on sources that allows for an in-situ oxide to be grown on both surfaces for passivation without diffusion glass removal [7]. All cells received a light phosphor emitter (80-120 $\Omega/\text{sq.}$) and transparent boron BSF (110 $\Omega/\text{sq.}$) during the same furnace process at 925°C with a 200Å in-situ oxide grown for passivation. Cells were measured immediately following a 15 minute FGA at 400°C and then subsequently degraded for 20 hours at \sim one sun and re-measured. Solar cells of varying thickness were fabricated on 0.7 Ωcm Cz-Si with 11 ppma O_i , using the above process. Their internal quantum efficiencies were measured using an OL Series 750 Automated Spectroradiometric Measurement System from Optronic Laboratories, Inc. both before and after light-induced degradation. Detailed analysis of measured IQE was performed to obtain bulk lifetime before and after LID and the front and back surface recombination velocity of these cells.

Modeling

Following extended IQE analysis [8], the degraded and un-degraded cells were modeled using the one-dimensional device modeling program PC1D [9]. The results of the extended IQE analysis suggested the following parameters be used in PC1D simulation: $R_b = 70\%$, $\tau_{\text{un-degraded}} = 75 \mu\text{s}$, $\tau_{\text{degraded}} = 20 \mu\text{s}$. The measured front surface reflectance of these cells was imported into PC1D so the calculated IQE could be compared directly to the measured IQE. In addition, external doping profiles were used for both the phosphorus emitter and boron back surface field. Using these parameters, IQE curves calculated by PC1D closely matched the measured IQE curves at the middle wavelengths. Surface recombination velocities were determined by fitting the calculated short and long wavelength IQE curves with the measured data. Short wavelength IQE was reliably matched to measurements from several samples using $S_F = 25,000 \text{ cm/s}$, but long wavelength IQE was slightly variable from sample to sample. These variations introduced some noise into the data, but were not enough to mask the trend toward less degradation in thinner samples. $S_R = 30,000 \text{ cm/s}$ proved to be a good worst-case value while simultaneously matching all samples well. Finally, the equivalent circuit element parameters were selected based upon the results of dark I-V analysis. The dark I-V results were difficult to fit, however, and so were used only as a starting point. N_2 was adjusted slightly to obtain the desired V_{OC} , while R_S was adjusted to obtain the desired fill factor. The final parameters were $R_S = 0.3 \Omega$, $R_{SH} = 84,745 \Omega$, $J_{02} = 15 \text{ nA}$, $N_2 = 1.75$. Using these parameters and a PC1D Quick Batch file, degraded and un-degraded devices were simulated and plotted side-by-side to show that thin cells suffer less from light-induced degradation than thick cells do. Further modeling was performed to determine the

optimum thickness that would result in highest stabilized cell efficiency and significantly reduced LID.

Results and Discussion

a.) Characterization and Analysis of Cell Data Before and After LID

Table 1 shows the change in solar cell parameters between the initial measurement before degradation and the final measurement after the degradation. Degraded stable efficiencies for all samples ranged between 15.3% and 14.8%. It is very apparent that

Table 1. LID in V_{oc} , J_{sc} , and Efficiency

Cell ID	Thickness	ΔV_{oc}	ΔJ_{sc}	ΔFF	ΔEff
Cz1n-1-2	378 μm	12.18	1.03	0.000	0.75
Cz1n-2-2	330 μm	8.92	0.81	-0.002	0.57
Cz1n-3-2	254 μm	10.55	0.51	-0.002	0.49
Cz1n-4-2	187 μm	6.61	0.02	-0.001	0.15
Cz1n-5-2	157 μm	7.88	0.19	-0.002	0.24
Cz1n-6-2	122 μm	2.73	0.07	0.000	0.10

Table 2. Stabilized Cell Performance after 20 Hours of Light Exposure

Cell ID	Thickness	V_{oc}	J_{sc}	FF	Eff
Cz1n-1-5	378 μm	618	31.19	0.773	14.9
Cz1n-2-2	330 μm	617	30.85	0.780	14.8
Cz1n-3-2	254 μm	619	31.47	0.786	15.3
Cz1n-4-5	187 μm	619	31.25	0.791	15.3
Cz1n-5-2	157 μm	619	31.18	0.787	15.2
Cz1n-6-6	122 μm	614	30.78	0.789	14.9

LID is reduced as the cell thickness is decreased. Table 2 shows the experimental stabilized cell efficiencies for each thickness. The stabilized cell efficiency peaks for the 150-190 μm thick samples. This is explained by the fact that the change in lifetime is directly related to the trap density N_t , which should be independent of thickness. However thinner cells with reasonable BSRV are less sensitive to lifetime degradation as long as the diffusion length is comparable or greater than the cell thickness. This is supported by Model calculations in Fig. 1 which shows that for the observed degradation in τ (from 75 μs to 20 μs), the 400 μm thick cell loses ~0.8% absolute in efficiency while the 150 μm sample loses ~0.3%

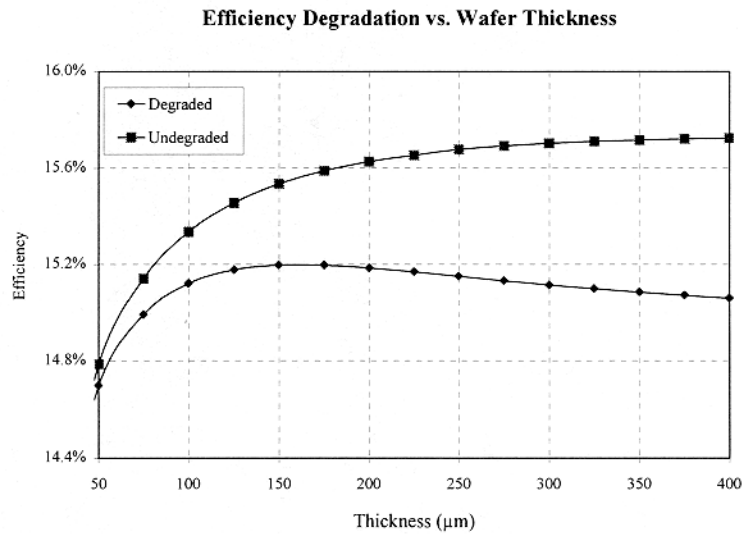


Figure 1. PCID modelling curve showing the effect of LID as a function of thickness. Top line is the un-degraded state ($t=75\mu s$) and the bottom line is the degraded state ($t=20\mu s$).

absolute in efficiency. These values match well with the experimental data in Table 1.

b.) Characterization and Analysis of IQE Before and After LID

IQE of each cell was measured before and after the LID. Match-up of the measured and calculated IQE gave a bulk lifetime of $75\mu\text{s}$ and $20\mu\text{s}$ before and after the degradation, with a BSRV of $30,000\text{ cm}^2/\text{s}$ for these cells. As expected, the long wavelength response is decreased for degraded solar cells. Figure 2 shows the measured loss in IQE of the samples in Table 1 in the long wavelength range due to the LID. It is readily apparent that the thin solar cells do not suffer as much current loss due to the degradation as the thick solar cells do. As the thickness decreases so does the effect of the lifetime degradation on J_{sc} and cell efficiency. The trend is also supported by the model calculations in Figure 3 for the thick and thin cells with lifetime degradation from $75\mu\text{s}$ to $20\mu\text{s}$.

c.) Thickness Optimization for the Highest Stabilized Efficiency After LID

Model calculations in Figure 4 show that the thinner the device, the smaller the LID effect on efficiency. However, absolute value of light induced efficiency degradation is also a strong function of BSRV. At a given thickness the higher the BSRV the smaller the LID. Nevertheless, this does not mean that higher BSRV is better, because the increased BSRV lowers the overall cell efficiency before and after the LID. The true figure of

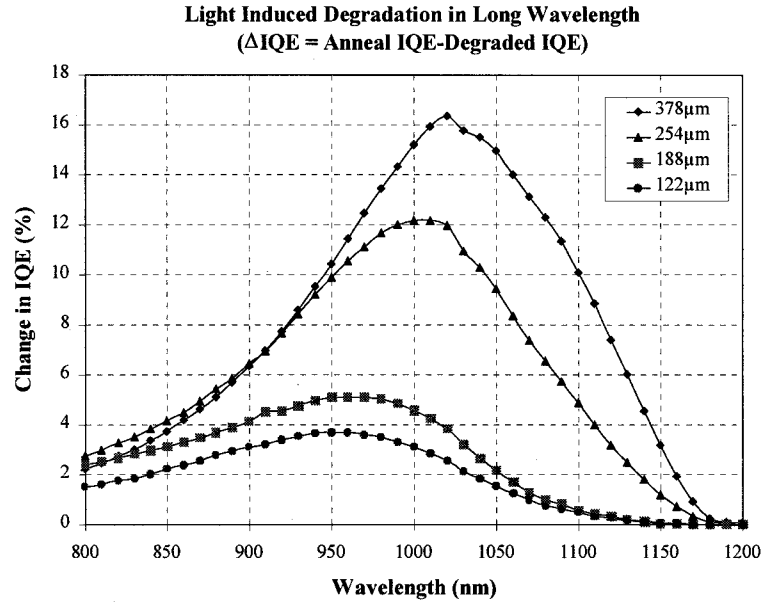


Figure 2. Measured LID in IQE in the long wavelength range for cells with varying thickness.

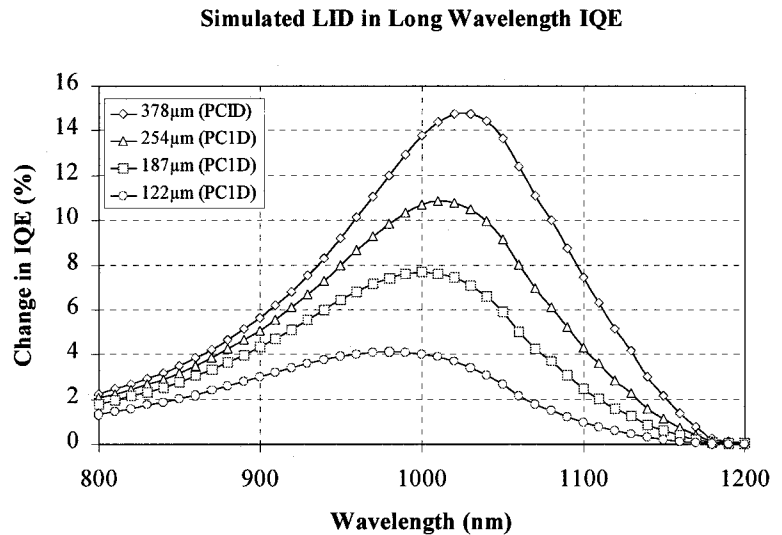


Figure 3. PC1D calculation showing LID in IQE in the long wavelength range for cells with varying thickness.

merit should be the stabilized cell efficiency after the degradation. Model calculations in Figure 5 shows that there is an optimum thickness which maximizes the stabilized efficiency for devices with good BSRV ($\leq 10^4 \text{ cm/s}$). It is important to note that for this Cz material and cell design, where lifetime degraded from $75\mu\text{s}$ to $20\mu\text{s}$ and a BSRV $\sim 10^4 \text{ cm/s}$, the optimum thickness for the highest stabilized efficiency is $\sim 150\mu\text{m}$. Reducing the thickness below that value further reduces the light induced efficiency degradation (Fig. 4) but it also lowers the stabilized cell efficiency (Fig. 4), which is the true figure of merit to assess the impact of LID effect on efficiency or power output. Figure 4 also shows that devices with very high BSRV (10^6 cm/s) require thicker material for the highest stabilized efficiency, which not only increases cost but gives lower absolute efficiency

Conclusion

This paper shows a methodology to reduce LID and optimize stabilized cell efficiencies for B doped Cz solar cells by controlling the cell design parameters. Reducing the cell thickness from $378\mu\text{m}$ to $157\mu\text{m}$ reduces the LID effect on efficiency and a higher stabilized efficiency is realized from 15.2% compared to 14.8%, Table 2. Modeling and experimental results show that thinner materials have a smaller efficiency drop caused by LID. Light induced efficiency degradation is also shown to be a function of BSRV, higher BSRV results in lower LID but it also lowers overall cell efficiency. This paper shows that the optimum thickness can be calculated from the LID of minority carrier and the BSRV of the cells. For the Cz material used in this study, the optimum cell thickness was found to be $\sim 150\mu\text{m}$ which gave the highest stabilized efficiency and significantly lowers light induced efficiency degradation (0.24%) while also lower production costs

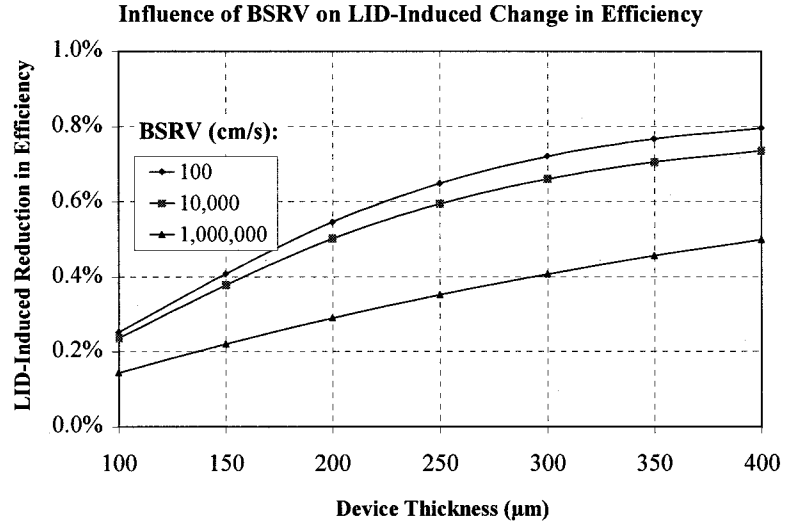


Figure 4. PC1D modeling curve of BSRV effect on the efficiency degradation due to LID trap formation in Cz Si solar cells as a function of thickness.

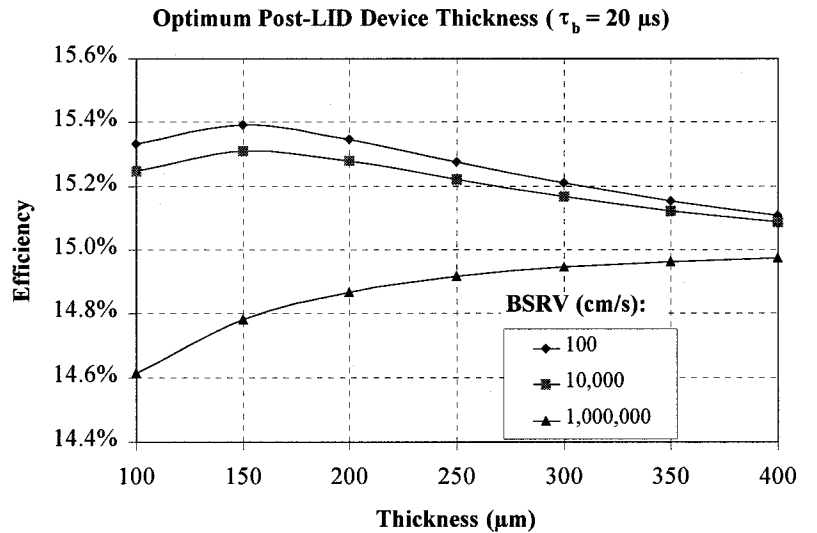


Figure 5. PC1D modeling curve of BSRV effect on the optimum efficiency of light degraded Cz Si solar cells as a function of thickness on finished solar cells.

[10]. Efficiency degradation was reduced from 0.75% to 0.24% when the cell thickness was reduced from 378 to 157 μ m. Reduction in cell thickness by more than a factor of two also significantly reduces the cost of solar cells.

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Copper precipitate dissolution in silicon

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The dissolution of copper precipitates in silicon has been studied with synchrotron-based x-ray fluorescence. Copper has been intentionally introduced and allowed to precipitate at oxygen precipitates and growth-related stacking faults. The dissolution of copper precipitates has been monitored after low temperature anneals with synchrotron-based x-ray fluorescence. This study is designed to determine whether or not copper can be released from precipitation sites at low temperatures such that the copper could then be removed from solar cell silicon. Our results demonstrate copper dissolution occurs at temperatures as low as 360°C and rapid dissolution at elevated temperatures. However, full dissolution does not occur in all cases studied here. These results indicate copper can be removed rapidly from solar cell silicon even with low temperature processing, however, some precipitated copper will remain behind and act as carrier recombination sites.

INTRODUCTION

Transition metal contamination of silicon is of significant concern in the photovoltaic industry. Transition metals can be easily introduced from stainless steel and copper tools during ingot growth and processing. The metal impurities can exist in a dissolved or precipitated state within the silicon, both of which produce deleterious effects. Dissolved transition metals can form deep levels, which enhance carrier recombination and generation while precipitated impurities form energy bands, which enhance recombination, generation and can create electrical shorts. These undesirable properties can be induced by even trace amounts of impurities, on the order of parts-per-trillion (ppt), if these trace impurities are left precipitated. In photovoltaic manufacturing, impurity concentrations can be found up to parts-per-million (ppm). Therefore, it is highly desirable to maintain low levels of metal impurities and to avoid impurity precipitation within the active device region, which for photovoltaic devices is typically the entire thickness of the solar cell, 300-500µm.

Removal of impurities, known as gettering, from active device regions of photovoltaic silicon is typically performed with phosphorus or aluminum gettering on the front and backside of the solar cell ^{1,2}. These gettering techniques are classified as extrinsic or external gettering since the mechanism for gettering is extrinsic to the original material. Both phosphorus and aluminum gettering are inherent for solar cell processing and do not require significant variations to processing steps.

Since Cu has the highest diffusivity and solubility of transition metals in silicon ³ and Cu is commonly found in many forms of processing equipment, the removal of Cu from solar cell silicon is of particular interest. Furthermore the high diffusivity of Cu allows for rapid precipitation during cooling or a later, lower temperature heat treatment. This rapid precipitation allows for even part-per-trillion concentrations to easily precipitate and thus form performance limiting defects in the solar cell.

In this work we present a study of copper precipitate dissolution in single crystal silicon with oxygen precipitates and their growth-related defects. Specifically, dissolution of copper precipitates at low temperatures in an effort to simulate the thermal budgets found in the aluminum sintering process of solar cell manufacture. Single crystal silicon with oxygen precipitates was used in order to provide the most stable state of copper in silicon in order to test the worst-case scenario for copper removal from solar cell silicon. Copper oxides are significantly more stable than other possible forms of copper precipitates in silicon, such as metallic copper and copper silicide. While copper oxide formation has not been observed in silicon with oxygen precipitates, we wanted to

provide the opportunity for copper oxide formation. Using X-Ray Fluorescence (XRF) at the Advanced Light Source, Lawrence Berkeley National Laboratory we have the ability to detect nm-scale metal precipitates with $1\text{-}2\mu\text{m}^2$ spatial resolution and scan areas typically hundreds of square microns. This technique provides orders of magnitude higher sensitivity with a high sampling volume compared to typical characterization techniques such as: Energy Dispersive Spectroscopy, Secondary Ion Mass Spectroscopy, Auger Electron Spectroscopy or Transmission Electron Microscopy.

EXPERIMENTAL

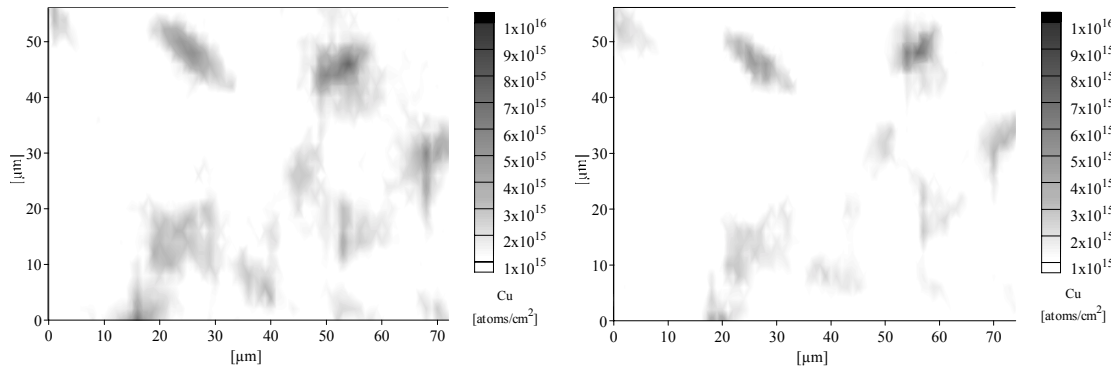
Boron-doped single crystal Czochralski (CZ) silicon was used in this work. The dissolved oxygen concentration was 10^{18} atoms/cm³, as measured by Fourier Transform Infrared spectroscopy (FTIR). The CZ silicon was subjected to a series of heat treatments to produce an oxygen precipitate density of 10^{11} precipitates/cm³ and a stacking fault density of $\approx 10^5/\text{cm}^3$. Descriptions of the precipitate-forming heat treatments are given in ⁴. Cu was intentionally introduced in the CZ material by dip-coating the samples in a solution of copper fluoride tri-hydrate, HF and H₂O followed by a 1170°C in-diffusion performed in a N₂ ambient. The anneal times used in these experiments were more than sufficient to establish the equilibrium concentration of 10^{18} Cu atoms/cm³ throughout the thickness of the material. The samples were air-cooled. No dissolved Cu was detected with Transient Ion Drift (TID) measurements, which has a sensitivity of 10^{11} Cu atoms/cm³. The slow cool allowed for Cu precipitation at the oxygen precipitates and stacking faults. Excess Cu was removed from the surface by mechanical polishing and chemical etching. Anneals to dissolve the Cu precipitates were performed at 360°C and 460°C for 30 minutes in a quenching furnace with a quench rate of 1000°C/sec. The quench halts the dissolution process and inhibits the re-precipitation of the Cu. Prior to analysis, the surfaces of all materials were cleaned with a VLSI grade piranha (H₂SO₄:H₂O₂) etch, VLSI grade HF dips and >13 MΩ-cm resistivity water in a class 100 clean room.

For copper detection, we utilized synchrotron-based x-ray fluorescence (XRF) with which we ascertained spatial distributions of copper in the silicon. Beamline 10.3.1 at the Advanced Light Source, Lawrence Berkeley National Laboratory allows for micron-scale XRF analysis. For copper in silicon, the escape depth is on the order of 80μm. The sensitivity limit for Cu in silicon is 0.5 ppm, which means the μ-XRF system has the capability to detect one Cu precipitate with a 10nm radius or greater within a sampling volume of 80μm³. The sample stages can be scanned, allowing for large sampling areas. Details of the system are given in ^{5,6}.

RESULTS AND DISCUSSION

Using the μ-XRF system, we have identified the positions of Cu precipitates with reference to an intentional scribe mark on two samples. The elemental map taken on the first sample is shown in Figure 1. The density of the Cu clusters corresponds well with the stacking fault density of $10^5/\text{cm}^3$. Furthermore, the orientation of the Cu clusters is similar to the preferred orientation for stacking faults in silicon, where stacking faults prefer to lie on the (111) plane. We then annealed the sample at 360°C for 30 minutes in an attempt to dissolve the Cu precipitates. After annealing, the sample was re-scanned with the μ-XRF system in the same area using the scribe mark as a fiducial point. As shown in Figure 2, we observe a decrease in the amount of Cu at the clusters. However, all precipitates remain, indicating the 360°C anneal was insufficient to fully dissolve the Cu precipitates.

For the second sample we attempted to dissolve the Cu precipitates using a higher temperature anneal at 460°C. The μ-XRF maps of the sample in the initial state and after the 460°C anneal are shown in Figure 3 and 4, respectively. We observe more



Figures 1a&b: a) Precipitated Cu in CZ silicon with oxygen precipitates and stacking faults as measured with μ -XRF. b) Cu distribution after the sample has been annealed at 360°C for 30 minutes. Note that some of the Cu clusters have decreased in size and intensity.

dissolution of the Cu precipitates with the 460°C anneal as compared to the 360°C anneal. Some clusters have dissolved to below the μ -XRF sensitivity limit while others have significantly decreased in size and intensity.

The rapid dissolution of Cu at low temperatures indicates that Cu precipitated at stacking faults is unstable, such that the Cu may be introduced into the active device region during low temperature annealings. These low temperature anneals are commonly used in IC processing after the Cu metallization step and even during device operation.

Assuming Cu is in the form of Cu_3Si precipitates, theoretical calculations,^{7,8} predict a Cu_3Si precipitate with a radius smaller than 9nm and 70 nm would fully dissolve for 30 minute anneals at 360 and 460°C, respectively.

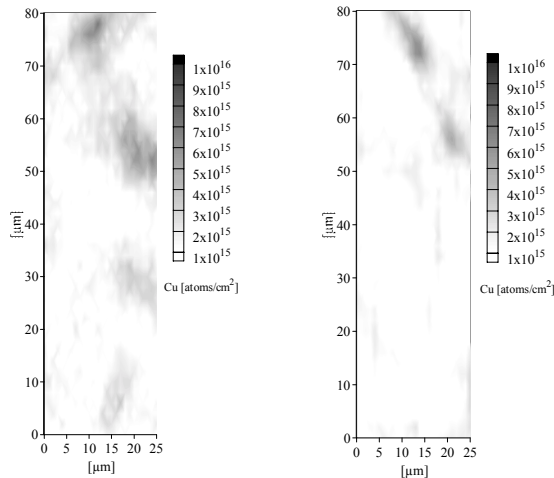


Figure 2a&b: a) Precipitated Cu in CZ silicon with oxygen precipitates and stacking faults as measured with μ -XRF. b) Cu distribution after the sample has been annealed at 460°C for 30 minutes.

temperatures. Other TEM studies^{11,12} provide an alternative possibility to enhanced Cu precipitate stability. These works identified the formation of CuSi rather than Cu_3Si for Cu precipitation in silicon and at the silicon surface. CuSi would be expected to have a slightly different dissolution rate than Cu_3Si , however, not as great of a difference as would be found for a Cu oxide compound.

In summary, we have presented results indicating Cu precipitates in silicon possess moderate stability at treatments as low as 360 or 460°C. These results imply that Cu can

Considering we do not observe full dissolution of all Cu clusters in this study, some Cu precipitates may be larger than 70 nm. However, considering the large strain field associated with Cu_3Si formation⁹ it seems unlikely such large precipitates would have formed. An alternative explanation is that the Cu precipitates are in a more stable form than Cu_3Si . Past transmission electron microscopy (TEM) studies on precipitated Cu in silicon by Solberg and Seibt^{9,10}, identified the formation of Cu_3Si when Cu was allowed to precipitate in silicon. However, these works were performed on silicon material without oxygen precipitates. The presence of oxygen precipitates may allow for the formation of Cu oxides, which are highly stable and would dissolve extremely slowly at low

be introduced into the active device region during low temperature anneals. The moderate level of stability indicates the Cu precipitates are not in the form of Cu_3Si but rather a more stable chemical state perhaps related to an oxide form.

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Modeling of Au outdiffusion from Si due to Al gettering

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ABSTRACT

Experiments and modeling of Au indiffusion in Si in the literature have shown that the indiffusion process is dominated by the Kick-Out (*KO*) mechanism, involving the interaction of Au atoms with Si self-interstitials (*I*). Our experiments and modeling of Au outdiffusion from Si due to Al gettering indicate that the outdiffusion of Au is dominated by the Frank-Turnbull (*FT*) mechanism, involving the interaction of Au atoms with vacancies (*V*).

1. Introduction

Aluminum gettering is a promising technology for improving performance of crystalline Si solar cells by removal of metal impurities from the Si [1]. For proper application of Al gettering, it is important to understand and accurately model the impurity diffusion and gettering processes. The diffusion behavior of Au in Si has been extensively studied [2-4] and makes it an ideal impurity for studying Al gettering.

Gold is a substitutional-interstitial impurity in Si, i.e., nearly all Au atoms reside on substitutional sites (Au_s), but diffusion occurs through fast-moving interstitial Au atoms (Au_i). Interchange between Au_s and Au_i needs participation of the native point defects in Si, viz., *I* and/or *V*. Thus, Au diffusion tends to create non-equilibrium concentrations of *I* and *V*. In dislocation-free Si, these non-equilibrium concentrations can be relaxed only by diffusion to or from free surfaces, which are infinite sinks or sources of *I* and *V*. Indiffusion of Au into dislocation-free thin Si wafers yields characteristic U-shaped profiles even when the Au source is on only one side of the wafer. Fast-diffusing Au_i easily diffuse through the wafer thickness, but incorporation of Au into substitutional sites is controlled by proximity to wafer surfaces rather than by proximity to the Au source.

Modeling and experiments in the literature have shown that Au indiffusion is dominated by the *KO* mechanism [2-4], wherein an Au_i yields an Au_s and an *I* or the reverse:



Thus, indiffusion of Au leads to generation and supersaturation of *I*, which is relieved by outdiffusion of *I* to the wafer surfaces. The competing *FT* mechanism [5] does not have much contribution during Au indiffusion. Here, an Au_i combines with a *V* to give an Au_s or the reverse:



Indiffusion of Au would lead to consumption and undersaturation of *V*, which would be relieved by indiffusion of *V* from the wafer surfaces.

Earlier modeling of Al gettering of Au assumed that the *KO* mechanism also dominated Au outdiffusion. This implies that outdiffusion of Au to the gettering layer would be controlled by proximity to the wafer surfaces. Outdiffusion of Au would lead to undersaturation of *I*, which would have to be relieved by indiffusion of *I* from the wafer surfaces. Even with an Al gettering layer on only one surface, the outdiffusion of Au would proceed to progressively greater depths from both surfaces as diffusion of Au_i

species to the Al gettering layer would not be the limiting process. Experimental results on Al gettering of Au in Si have been previously obtained by us [6], which qualitatively support these modeling results. Qualitatively speaking, the same phenomenon would be seen for the *FT* mechanism as well, with outdiffusion of supersaturated *V* controlling Au gettering. The purpose of this work was to quantitatively fit our experimental data.

2. Modeling

For modeling of gold diffusion simultaneously by the *KO* and *FT* mechanisms, the *I-V* reaction must also be taken into account :



where, ϕ represents a Si atom on a lattice site. The complete set of coupled, 1-dimensional partial differential equations to describe the Au diffusion process is [2,4] :

$$\frac{\partial C_s}{\partial t} = k_b^{KO} C_i^{eq} \left(\frac{C_i}{C_i^{eq}} - \frac{C_s}{C_s^{eq}} \frac{C_I}{C_I^{eq}} \right) + k_b^{FT} C_i^{eq} C_V^{eq} \left(\frac{C_i}{C_i^{eq}} \frac{C_V}{C_V^{eq}} - \frac{C_s}{C_s^{eq}} \right), \quad (4)$$

$$\frac{\partial C_i}{\partial t} + \frac{\partial C_s}{\partial t} = \frac{\partial}{\partial x} \left(D_i \frac{\partial C_i}{\partial x} \right), \quad (5)$$

$$\frac{\partial C_I}{\partial t} - k_b^{KO} C_i^{eq} \left(\frac{C_i}{C_i^{eq}} - \frac{C_s}{C_s^{eq}} \frac{C_I}{C_I^{eq}} \right) - k_b^{IV} C_I^{eq} C_V^{eq} \left(1 - \frac{C_I}{C_I^{eq}} \frac{C_V}{C_V^{eq}} \right) = \frac{\partial}{\partial x} \left(D_I \frac{\partial C_I}{\partial x} \right), \quad (6)$$

$$\frac{\partial C_V}{\partial t} + k_b^{FT} C_i^{eq} C_V^{eq} \left(\frac{C_i}{C_i^{eq}} \frac{C_V}{C_V^{eq}} - \frac{C_s}{C_s^{eq}} \right) - k_b^{IV} C_I^{eq} C_V^{eq} \left(1 - \frac{C_I}{C_I^{eq}} \frac{C_V}{C_V^{eq}} \right) = \frac{\partial}{\partial x} \left(D_V \frac{\partial C_V}{\partial x} \right), \quad (7)$$

where, C_i, C_s, C_I, C_V are the concentrations of Au_i, Au_s, I, V species respectively with the superscript "eq" representing the corresponding equilibrium concentrations. C_i^{eq} is taken to be 1% of C_s^{eq} . D_i, D_I, D_V represent the corresponding diffusivities with the species Au_s having negligible diffusivity, while k_b^{KO} , k_b^{FT} and k_b^{IV} represent the backward reaction rate constants of the *KO*, *FT* and *IV* reactions respectively, which are kept large enough to ensure dynamic equilibrium of the respective reactions. If only the *KO* mechanism is to be modeled, Eqns. (4)-(6) are used with k_b^{FT} and k_b^{IV} set to zero and if only the *FT* mechanism is to be modeled, Eqns. (4), (5) and (7) are used with k_b^{KO} and k_b^{IV} set to zero. The Al gettering process is accounted for by a suitable boundary condition, whereby dynamic equilibrium is maintained at the boundary between the Si and the Al at all times for Au [6] :

$$\left. \frac{C_i}{C_{Al}} \right|_{Si/Al} = \frac{C_i^{eq}}{C_{Al}^{eq}}, \quad (8)$$

where C_{Al} is the Au concentration in the Al and is assumed to be uniform through the thin Al layer thickness X_{Al} . The Au concentration in the Al increases as gettering proceeds, which is accounted for by increasing C_{Al} as per [6] :

$$\frac{dC_{Al}}{dt} = -\frac{D_i}{X_{Al}} \frac{\partial C_i}{\partial x} \Big|_{Si/Al}, \quad (9)$$

where the flux $\partial C_i / \partial x|_{Si/Al}$ is computed at the *Si/Al* boundary on the Si side.

3. Results

The experimental work consisted of Au indiffusion at $950^\circ C$ for 16 h into 530μ thick *FZ* Si, an etch to remove 15μ from both sides of the wafer samples and Al gettering at $1000^\circ C$ for 30 min with a 1μ thick Al layer on only one surface [6]. The Au outdiffusion profile measured by Spreading Resistance Profiling (*SRP*) is truncated about 50μ from both surfaces as the surface concentration of Au was too low to measure by *SRP*. Fig. 1 shows the fitting of the experimental profile by the *KO* mechanism alone. The gettering/outdiffusion process is too slow for normal values of $D_i C_i^{eq}$, and this value needs to be increased 10 times to get a reasonable fit. Fig. 2 shows the fitting by the *FT* mechanism alone where it is seen that a normal value of $D_V C_V^{eq}$ gives a satisfactory fit even when the individual D_V and C_V^{eq} values are varied over a few orders of magnitude. Fig. 3 shows the fitting by the *KO* and *FT* mechanisms together, which is very close to the fit by the *FT* mechanism alone.

4. Discussion

Since the value of $D_i C_i^{eq}$ is well-established, the fit obtained by the *KO* mechanism alone is not reasonable, as it requires $D_i C_i^{eq}$ be increased by one order of magnitude. In contrast, the *FT* mechanism gives a good fit to the experimental profile with a value of $D_V C_V^{eq}$ close to established values in the literature. Even though the $D_V C_V^{eq}$ value is very close to the $D_i C_i^{eq}$ value at the temperature in question, the *FT* mechanism clearly has a dominant contribution to Au outdiffusion, in direct contrast to the domination of the *KO* mechanism for Au indiffusion at the same temperature. Vacancies get supersaturated during Au outdiffusion, and the diffusion of *V* to the surfaces limits Au outdiffusion or gettering.

5. Summary

Gold outdiffusion during gettering is controlled by the *FT* mechanism. Modeling by the *KO* and *FT* mechanisms combined clearly shows that the *FT* mechanism has a dominant contribution to Au outdiffusion.

6. Acknowledgements

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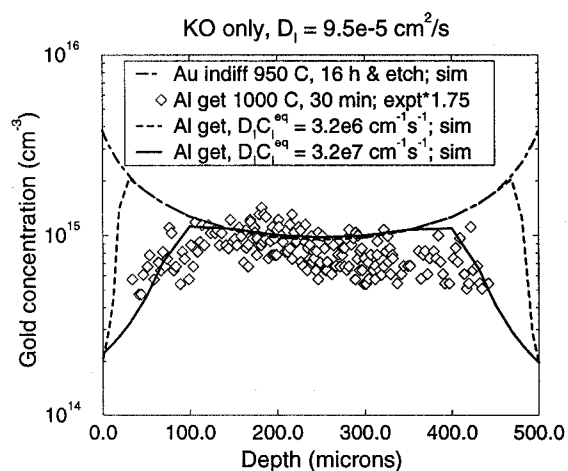


Figure 1. Fitting of experimental profile by KO mechanism only with two different values of $D_I C_I^{eq}$

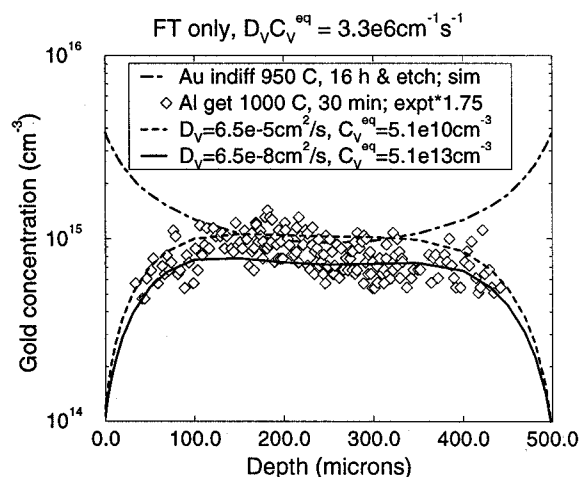


Figure 2. Fitting of experimental profile by FT mechanism only with $D_V C_V^{eq}$ kept constant and D_V varied.

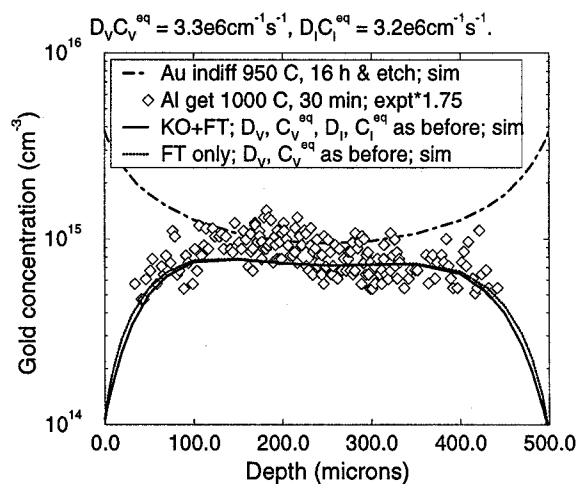


Figure 3. Fitting of experimental profile by KO and FT mechanisms combined.

Extremely High Currents in RGS (Ribbon Growth on Substrate) Silicon Solar Cells by 3D Carrier Collecting Channels

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Abstract

RGS (Ribbon Growth on Substrate) silicon could be the crystalline silicon material for PV of the future. Its very fast production technique avoiding any material losses due to sawing will drastically reduce the wafering costs. On the other hand one has to deal with more crystal defects (grain boundaries, dislocations, impurities) which limit especially the diffusion length L_{diff} and normally result in small short circuit current densities J_{sc} . The charge carrier collection probability can be increased by a macroscopic V-texture of the surface, but even more effective is a 3-dimensional emitter structure within the whole bulk cell volume. This was observed in RGS solar cells showing minority carrier lifetimes of only around 0.2-0.4 μs but J_{sc} of $>34 \text{ mA/cm}^2$. In these cells the whole bulk volume is collecting current despite of the small diffusion lengths.

This behaviour was investigated using spatially resolved IQE (Internal Quantum Efficiency) mappings, capacitance measurements and a special EBIC technique where the electron beam hits the backside of the wedge-shaped solar cell. From our results we conclude that the collecting structures may be caused by inversion in combination with the high O and C content. Cells with large areas of collecting channels exhibit lower fill factors (FF) but nearly no loss in open circuit voltage V_{oc} as compared to standard RGS cells. For both types of cells confirmed record efficiencies of 12.5% have been obtained.

Introduction

The Bayer RGS technique [1] could play a major role in a more cost effective production of multicrystalline Si wafers for PV. A decoupling of the directions of crystallisation and pulling leads to high pulling speeds of $\sim 10 \text{ cm/s}$ and therefore a production rate of $\sim 1 \text{ wafer/s}$. The fast process results in grain sizes $< 1 \text{ mm}$, dislocation densities of $10^5\text{-}10^7 \text{ cm}^{-2}$ and diffusion lengths $< 20 \mu\text{m}$ [2]. The high oxygen and carbon concentrations ($\sim 2 \cdot 10^{18} \text{ cm}^{-3}$ respectively) require special cooling techniques in order to avoid the formation of the so-called New Donors [3]. Therefore RGS material is currently produced in two forms which can be distinguished by their cooling rates after crystallisation [4,5].

- Using a very fast cooling rate allows the oxygen to remain in interstitial form. Subsequent process steps in the temperature range of 600-900 °C have to be avoided during solar cell processing.
- An annealing step $> 1000 \text{ °C}$ forms large oxygen precipitates and reduces the interstitial oxygen concentration by one order of magnitude. The formation of New Donors is now no critical issue anymore.

All cells investigated within this study have been processed using the latter cooling rate including the high temperature annealing step. During this step oxygen and carbon precipitates at crystal defects, especially at dislocations, which could be shown by TEM (Transmission Electron Microscopy). These precipitates may play the key role in the observed 3-dimensional emitter structure in RGS solar cells described in the following.

Solar Cell Process and IV-Data

The RGS solar cells have been processed following the sequence shown in Fig. 1. After a mechanical levelling step to flatten the surface and to remove segregated impurities a macroscopic V-texture was applied using a dicing saw with bevelled blades. This results in a lower reflectivity and a higher carrier collection probability as could be shown in previous studies [6,7]. After emitter formation, thermal oxide passivation and gettering/BSF formation an optimised H-passivation step using the MIRHP (Microwave Induced Remote Hydrogen Plasma) technique was applied.

Mechanical surface levelling
Defect etching
Mechanical V-texture
Saw damage etching
POCl ₃ emitter diffusion
Thermal oxidation
Al gettering
Hydrogen passivation
Front grid (Photolithography)
Full Al back contact
Cell separation (2x2 cm ²)

Fig. 1: Applied RGS solar cell processing sequence including a V-texturing and an optimised hydrogen passivation step.

Table 1: IV-data of the two best RGS solar cells within this study (cell size 4 cm², independently confirmed by JRC, Ispra).

Cell	V _{oc} [mV]	J _{sc} [mA/cm ²]	FF [%]	η [%]
1	549	34.5	65.9	12.5
2	560	31.1	71.6	12.5

The best cells received a ZnS/MgF₂ ARC (AntiReflection Coating) and the IV-data of all cells have been determined. Tab. 1 shows IV-parameters of the best two cells. Both cells show identical efficiencies of 12.5%, which is the highest value obtained on RGS material so far. Nevertheless J_{sc} and FF of both cells differ strongly. The extremely high J_{sc} value of cell 1 can not be explained assuming a planar emitter structure on the V-textured surface and lifetimes far below 1 μs as it is the case for RGS.

Results and Discussion

In Fig. 2 the spatially resolved IQE mappings at 905 nm reveal that in cell 1 large areas have exceptionally high values close to 1 whereas in cell 2 only a smaller fraction within the cell shows

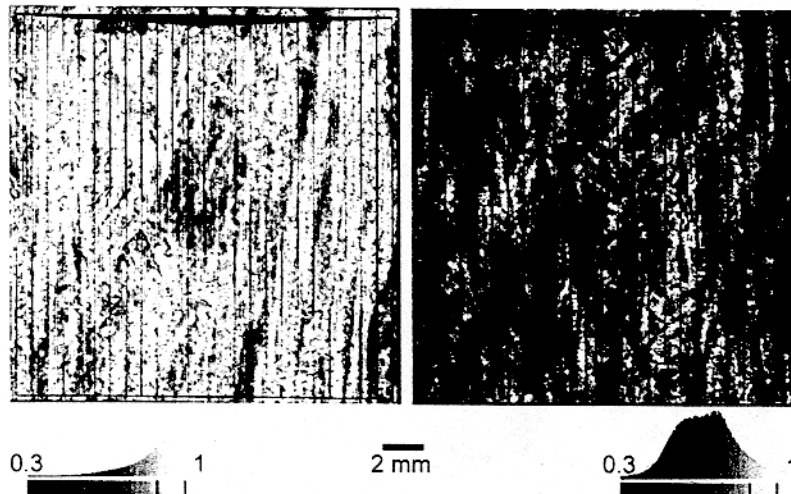


Fig. 2: IQE mappings (905 nm) of RGS cells 1 (left) and 2 (right). In cell 1 a large fraction of the cell shows exceptionally high IQEs whereas in cell 2 a mixture of high IQEs and the "normal" behaviour is visible.

this behaviour. In the rest of cell 2 “normal” values of the IQE can be seen, which are compatible with the measured low lifetimes.

Capacitance measurements have been carried out in order to study the nature of the current collecting structures. For all cells the capacitance was measured using a low frequency of 100 Hz (C_{LF}) and a high frequency of 100 kHz (C_{HF}). In Fig. 3 the difference of the signals $C_{LF} - C_{HF}$ is given in dependence on the cell parameters.

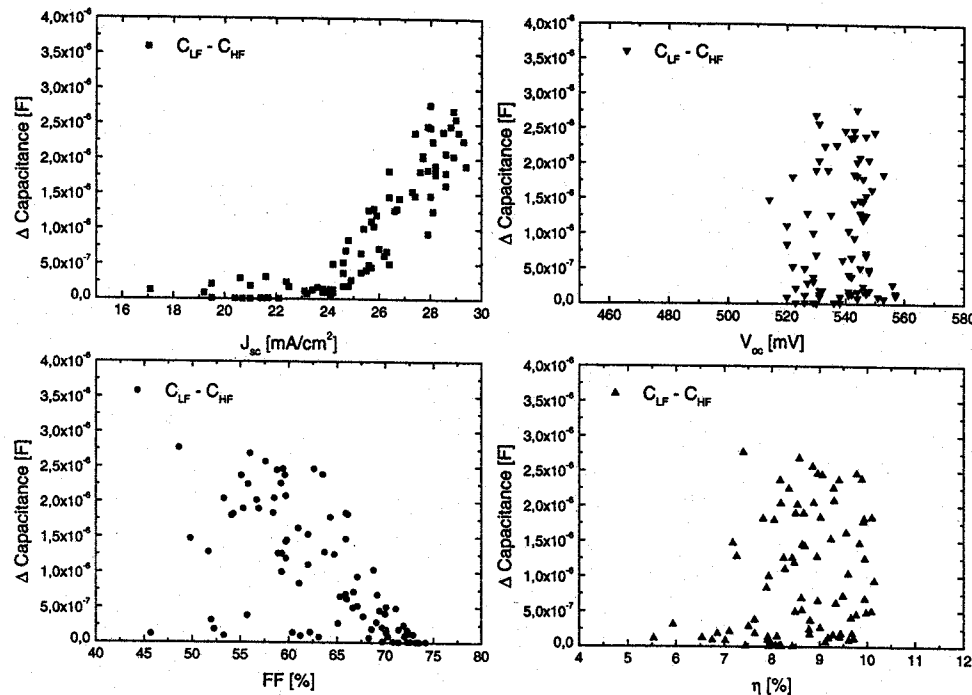


Fig. 3: $C_{LF} - C_{HF}$ of the processed RGS solar cells (4 cm^2) without ARC in dependence on the cell parameters. Especially J_{sc} and FF are affected.

A large difference of both capacities ($C_{LF} - C_{HF}$) indicates a slow charge carrier exchange which contributes only to C_{LF} and is typical for minority charge carriers. Therefore an inversion channel model was developed and published [5]. It is based on n-type channels along grain boundaries and/or dislocations which form an extension of the P-doped surface emitter into the p-type silicon bulk. Minority charge carriers in the bulk do not have to diffuse to the cell surface but are collected within the channels which are in contact with the surface emitter. If the typical distance between the channels is in the order of L_{diff} ($\sim 20\text{-}40 \mu\text{m}$ after cell processing) even carriers generated deeply in the bulk are collected.

The current collecting channels can be investigated by using a special EBIC technique. The electron beam hits the backside of the solar cell which was ground in a wedge-shape from the backside. In this way the Al back contact is removed and the electron beam penetrates into the silicon. Results from the EBIC investigation are presented in Fig. 4.

The density of the channels visible allows carriers generated deeply in the bulk to be collected very efficiently leading to the observed high J_{sc} . The presence of collecting channels presently lowers the FF as can be seen in Fig. 2. This might be due to shunting problems (n-type channels in contact with the Al backside metallization) and/or the fact that in forward (operation) direction the inversion channels act as preferred injection sites leading to enhanced leakage currents [5]. If these problems can be overcome, inversion channels may lead to higher efficiencies of RGS solar cells with small diffusion lengths.

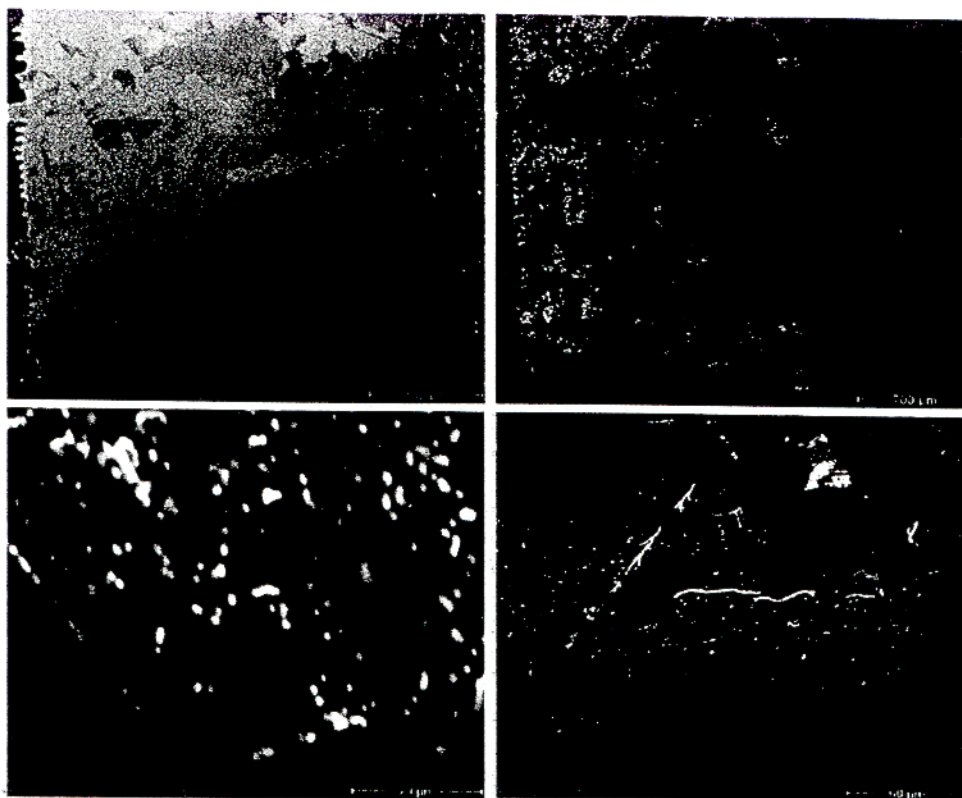


Fig. 4: EBIC investigation of a RGS cell showing an exceptionally high J_{sc} . **Top left:** SEM (Scanning Electron Microscope) picture (5 kV) of the wedge-shaped cell from the back. In the left part the thickness is zero, in the right part the remaining Al back contact is visible. **Top right:** EBIC image (5 kV) of the same area. Even in thick areas close to the back contact an efficient current collection is visible. **Bottom left:** Close-up of the top EBIC image resolving individual channels (5 kV). **Bottom right:** Cross section of the cell revealing the V-texture and the collecting channels within the whole bulk volume of the cell (2 kV).

Conclusion

12.5% efficient solar cells made from RGS silicon with small L_{diff} have been processed partly showing extremely high values of J_{sc} exceeding 34 mA/cm^2 . This behaviour can be explained by current collecting channels which form a 3-dimensional continuation of the front side emitter into the silicon bulk. These channels can be visualised by EBIC measurements and are most probably caused by segregation of impurities (O and/or C) at dislocations/grain boundaries during the high temperature annealing step after crystallisation. The microscopic/chemical explanation is unclear yet and has to be investigated further. Cells with collecting channels and an optimised hydrogen passivation show the same maximum efficiencies as compared to cells 'without' channels, but FF is lowered. If this is due to shunting problems between the channels and the cell back contact, avoiding a direct contact could further improve the efficiency of RGS cells containing channels.

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Application of synchrotron radiation-based X-ray fluorescence microprobe to detect impurities at the location of a shunt.

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Shunts are one of major defects limiting solar cell efficiency. They are local spots of low open circuit voltage that drain current from the areas with a higher open circuit voltage, thus decreasing the total output voltage of the cell and, consequently, their overall efficiency. Localization and identification of shunts in processed solar cells had remained a problem for a long time, until the technique of infra-red thermography was developed and applied to photovoltaics (see, e.g., [1-4]). This technique detects a local increase of temperature on the wafer (typically on the order of millikelvin or less) in the area where a current flows through the shunt. According to most of the authors, localized dislocations are not involved in shunt formation. Some of the local shunts were found associated with accumulation of grain boundaries, while others are defects of *pn*-junctions. The dominant shunts have often been found at the edges of the cells. The dependence of the shunt strength on elastic deformation of the cells, which is sometimes observed, indicates that mechanical stress may influence certain shunts. According to Breitenstein *et al.*, the quantitative influence of shunts on the efficiency is shown to increase to above 30% for illuminations below 0.2 suns. For stronger illuminations the effect may be weaker, but certainly not less than several percent of cell efficiency.

It was shown that shunts, localized by IR thermography, can also be observed as contrast spots in EBIC and LBIC maps. However, only few of recombination-active spots are shunts, and there is no simple way to tell from EBIC or LBIC measurements alone which of the contrasts is a shunt. Additionally, despite numerous efforts to identify the nature of the shunts, no consistent model is available yet. Some researchers believe that shunts are more process-related than inherent in the silicon material used for manufacturing of solar cells. However, the ultimate answer can be given only after a detailed research.

In this study, we applied the X-ray fluorescence microprobe technique to test whether metal impurities may be involved in the shunt formation. The measurements were performed at the Advanced Light Source, Lawrence Berkeley National Laboratory. Synchrotron-generated X-ray radiation was focused to a spot size of $1\text{-}2\text{ }\mu\text{m}^2$, with scan area typically over hundreds of microns. The sampling depth of the measurement was on the order of $10\text{-}80\text{ }\mu\text{m}$. Our previous analyses demonstrated that the μ -XRF system is capable of detecting metal precipitates with radii $> 20\text{ nm}$, which is superior to other standard characterization techniques such as SIMS, EDX, or Auger spectroscopy. The μ -XRF system detects fluorescent X-rays emanating from the material after excitation with a wide band pass, 12.4 keV energy X-ray beam. The energy of the fluorescent X-rays signifies the element present. The study was performed in collaboration with the colleagues from the Institute of Semiconductor Physics (Frankfurt-Oder, Germany), who provided us with material pre-characterized with infra-red thermography and EBIC. The location of a shunt was described by its position relatively to grain boundaries, visible also in optical microscope (see Figs. 1-5). This data were used to position the sample in the XRF system. The starting material for this study was a fully processed polycrystalline solar cell.

Preliminary EDX measurements performed in a scanning electron microscope revealed that the shunt could be caused by a particle containing gold. Even after prolonged treatment in aqua regia the *Au* containing particle could not be dissolved. So it was not clear if the particle is pure *Au* or a compound/silicide. The purpose of the XRF studies was to check whether shunt is indeed associated with gold, and if any other metal impurities are present at the shunt location. Unexpectedly, X-ray fluorescence studies resulted in a different conclusion: no gold was detected at the shunt location; however, a significant concentration of titanium was found.

Presently it is difficult to say what the reason of the discrepancy between the results of EDX and XRF in terms of the nature of the detected metal contaminant (*Au* vs *Ti*) are. We are now considering the possibility of obtaining a series of pre-characterized samples with shunts to perform a series of XRF measurements to determine if metal contamination at the shunt locations is reproducible. At this point we can only say that our experiment indicated that shunts are associated with metal contaminants, and that these contaminants are likely to be heavy metals such as titanium or gold. The hypothesis that shunts may be associated with titanium is physically plausible because Ti has a very low diffusivity in silicon, and cannot be efficiently gettering by non-proximity gettering techniques unless the gettering is performed for a long time at very high temperatures. Therefore, it should be very difficult to eliminate shunts from the solar cells by gettering.

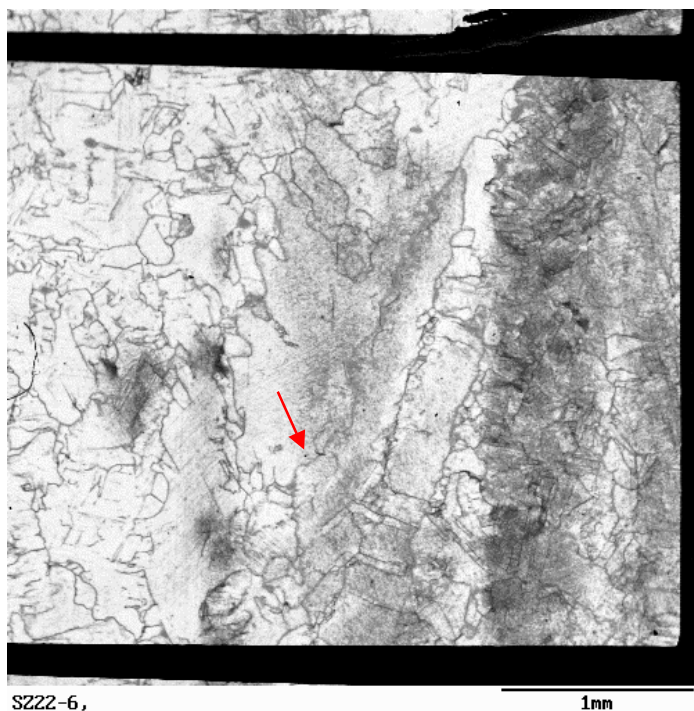
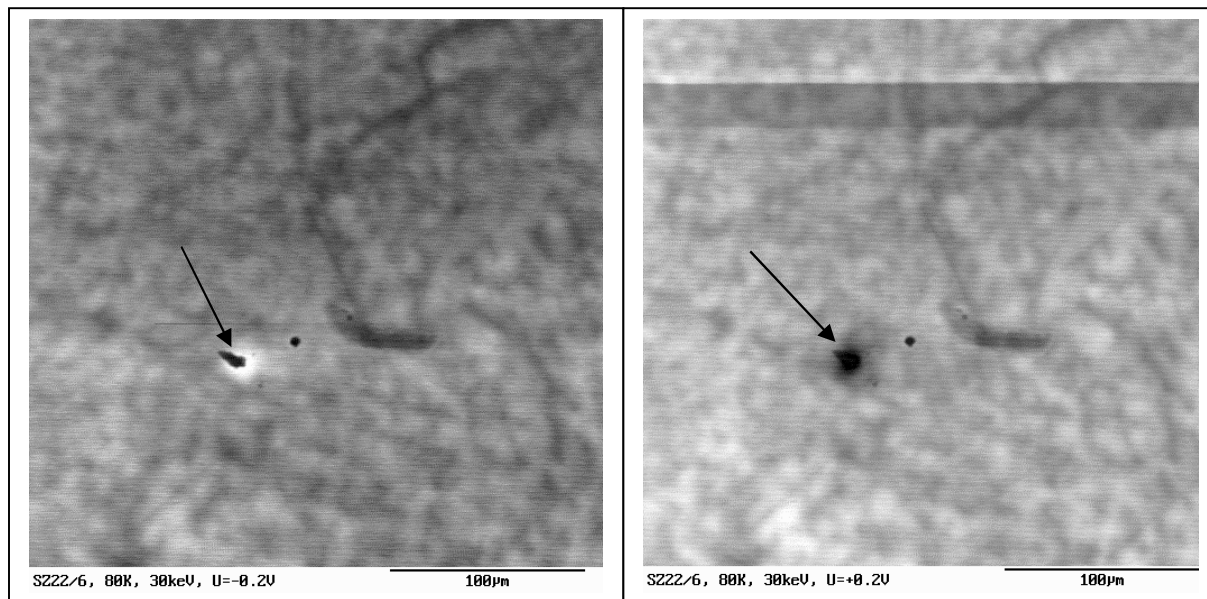


Fig. 1: EBIC images of the solar cell which was found by infra-red thermography to contain a shunt. Arrow indicates shunt position.

Figs 2, 3: EBIC images at reverse and forward bias, respectively. Contrast reversal is an indication of a missing p-n junction.



Figs 4, 5: Secondary electron images with different magnification showing the position of the shunt relative to grain boundaries and scratches on the sample. Dark arrows in Fig 5 mark scratches on the surface which were used to locate the shunt.

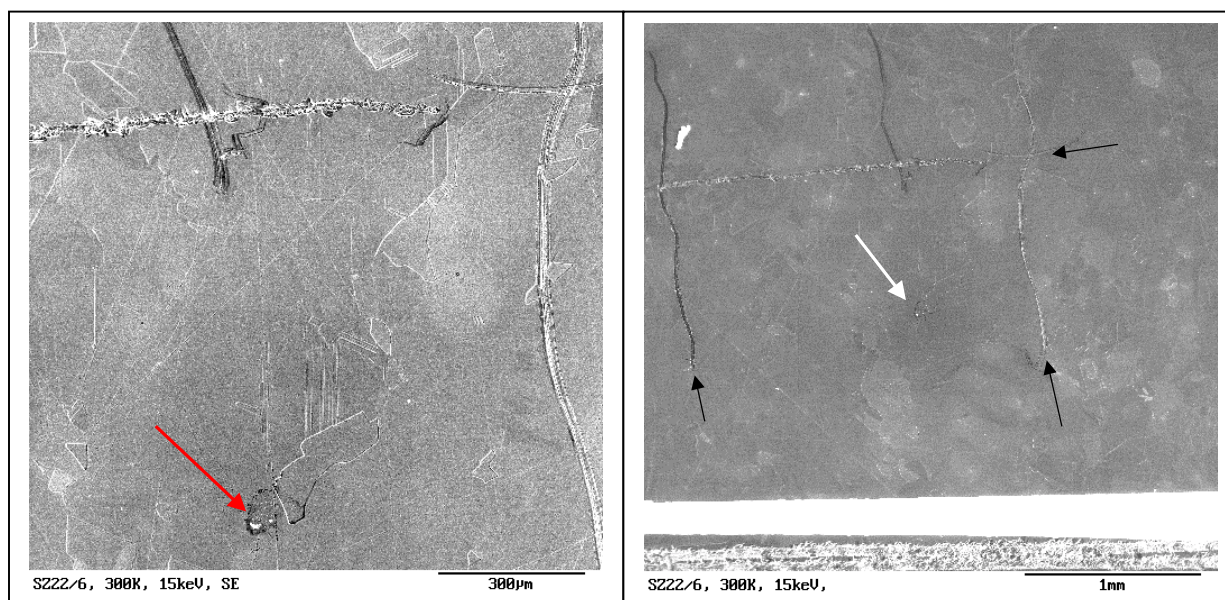
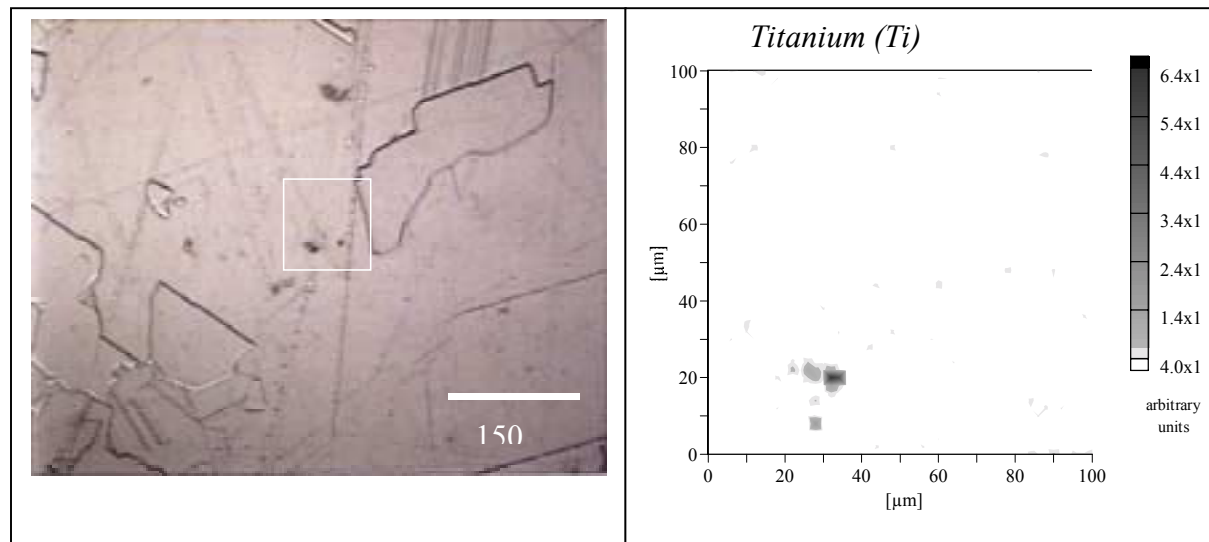


Fig. 6. 20X Optical image of the sample. White box denotes the XRF scan area.

Fig. 7. XRF map of Ti in the sample. The scan was performed within the area indicated by the white box in Fig. 6.



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Study of precipitation/outdiffusion of copper in CZ and EFG silicon wafers

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Copper possesses unique physical properties in silicon which are significantly different from all other impurities. This difference is primarily associated with the positive charge state of copper at both elevated and room temperatures [1]. The small ionic radius of ionized copper enables it to diffuse much faster than any other 3d transition metal, with the intrinsic diffusion barrier as low as 0.18 eV [2]. In *p*-type silicon, shallow ionized acceptors serve as trapping sites for Cu_i^+ and decrease the copper diffusivity to its effective diffusion coefficient, given at room temperature for *Cu* concentrations much lower than the doping level and for the silicon wafers with resistivity of $10 \Omega \times \text{cm}$ by $D_{\text{eff}}(293\text{K}) = 4.44 \times 10^{-8} \text{ cm}^2/\text{s}$ [2]. Using this diffusion coefficient, one can apply Ham's law [3], $\tau = (4\pi D_{\text{eff}} n r_0)^{-1}$, to calculate the expected precipitation time constant of copper in silicon with a known density of internal gettering sites.

In our experiments we used CZ silicon with pre-characterized density of oxygen precipitates varying in the range from 10^6 to 10^{11} cm^{-3} [4] and EFG multicrystalline material. Preparation of the silicon samples, their intentional Cu contamination, furnace anneal with subsequent quench in ethylene glycol, chemical cleaning, Schottky diode evaporation, and Transient Ion Drift (TID) measurements were performed using standard procedures, described in our previous publications (e.g., [2]). Parameters of the CZ wafers used in this study and the expected precipitation time constants τ , calculated from the Ham's law, were as follows:

Sample	$\Delta O_i (\times 10^{17} \text{ cm}^{-3})$	$N_{\text{oxy}} (\text{precip}/\text{cm}^3)$	radius ($\times 10^{-6} \text{ cm}$)	Expected τ (s)
Si6	<0.1 (below detection limit)	1.8×10^6	unknown	>10,000
Si7	<0.1 (below detection limit)	2.0×10^7	unknown	>4000
Si8	0.28	2.3×10^8	8.38	930
Si9	0.54	1.6×10^9	5.46	205
Si10	2.25	1.5×10^{10}	4.15	28.8
Si11	6.00	2.5×10^{11}	2.25	3.2

TID measurements of the interstitial copper concentration were performed after 30 min of room temperature storage of the samples – the time required to chemically clean the samples and fabricate Schottky diodes. If oxygen precipitates were effective precipitation sites for *Cu*, then one would expect the Cu_i concentration in the Si8 sample to decrease as compared to the equilibrium *Cu* solubility at the diffusion temperature by a factor of 7, while in the Si9 sample it would decrease by more than three orders of magnitude and will be close to the detection limits of TID. Finally, *Cu* would precipitate completely in the samples Si10 and Si11. On the contrary,

in the samples Si6 and Si7 with very slow precipitation rates the interstitial copper concentration can be expected to change by less than a factor of 2. The anticipated change in the precipitation rate by several orders of magnitude as the density of oxygen precipitates changed from 10^8 to 10^{11} cm^{-3} was observed in our earlier study of precipitation of iron in silicon [4]. This expectation, however, was not confirmed for copper.

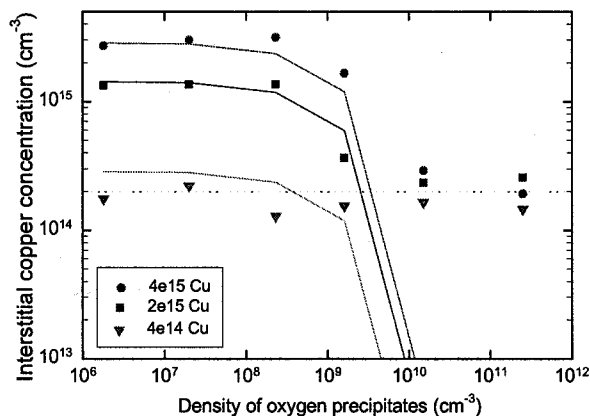


Fig. 1. Interstitial copper concentration detected by TID 30 min after the quench for samples with different densities of oxygen precipitates and different initial copper concentrations. The initial copper concentration, determined by the annealing temperature, is indicated in the inset. Solid lines are simulations based on the Ham's law. To achieve the best possible agreement with the experimental data, we had to assume that only 10% of the surface of oxygen precipitates getter Cu.

EBIC studies of CZ samples after copper diffusion clearly indicated that oxygen precipitates were decorated with copper, although the fraction of copper precipitated at oxygen precipitates could not be evaluated from EBIC measurements alone. The precipitation rate of copper measured by TID was much slower than expected from Ham's law, thus indicating that oxygen precipitates were poor gettering sites. Despite our expectation that the decay of the interstitial Cu_i concentration during the first 30 min of room temperature storage after the quench (this time was required to manufacture Schottky-diodes) should be a factor of 6.9 for the sample Si8, the experimentally observed decay for the Si8 sample was as low as a factor of 2 (see Fig. 1). For the sample Si9, the decay of copper concentration was less than a factor of four, although the

concentration decay predicted by Ham's law was about a factor of 6×10^3 (see the table above). Furthermore, in the samples Si10 and Si11, in which we expected the indiffused copper to precipitate completely within the first 30 min, the decay of the Cu_i^+ concentration was only given by a factor of 20 to 40. Additionally, the decay time of the remaining copper concentration as measured by TID was in agreement with the precipitation-free outdiffusion model. This implies that oxygen precipitates did not have any significant effect on the behavior of interstitial copper during measurements.

One could hypothesize that we observe the effect of saturation of oxygen precipitates with copper, whereby the oxygen precipitates become inefficient as soon as they getter a certain amount of copper. Indeed, EBIC analysis indicated an increase in recombination activity of oxygen precipitates caused by copper contamination. However, a comparison of TID data obtained on samples with different initial copper concentration (Fig. 1) suggests that the effect is more complicated. Obviously, precipitation of copper at oxygen precipitates depends not only on the density of the precipitates, but also on the initial copper concentration. For relatively high initial copper concentrations, $2 \times 10^{15} \text{ cm}^{-3}$ (circles in Fig. 1) and $4 \times 10^{15} \text{ cm}^{-3}$ (squares), gettering effect becomes appreciable only in the samples with the density of oxygen precipitates exceeding 10^8 cm^{-3} . In contrast, if the initial copper concentration is lower, $4 \times 10^{14} \text{ cm}^{-3}$ (green curve in Fig.

1), then there is no dependence of the Cu_i concentration detected by TID on the density of oxygen precipitates whatsoever, and likewise there is no appreciable gettering effect. An interesting feature of the Fig.1 is that the residual interstitial copper concentration, detected in the Si10 and Si11 samples in the beginning of the TID measurements, is almost independent of the starting copper concentration and is equal to about $2 \times 10^{14} \text{ cm}^{-3}$. This suggests that similarly to bulk precipitation of copper in FZ silicon [7], there is a critical copper concentration that should be reached to trigger precipitation of copper at oxygen precipitates. As soon as interstitial copper concentration drops below this critical value, precipitation of copper slows down or stops. Our data presented in Fig. 1 suggests that this critical concentration is about 2×10^{14} to $4 \times 10^{14} \text{ cm}^{-3}$ of copper in $10 \Omega \times \text{cm}$ silicon. Note that since interstitial copper is a shallow donor, increase of the Cu_i^+ concentration in the sample results in electrical compensation of the sample and a gradual upwards shift of the Fermi level. The critical compensation level observed in this study corresponds to the Fermi level position between approximately $E_V + 0.3 \text{ eV}$ and $E_V + 0.5 \text{ eV}$. This agrees with the expectation that the position of the energy levels of dislocations in silicon should be close to the mid-gap (see, e.g., Ref [5]). Indeed, it is known that oxygen precipitates tend to punch out dislocations, and that dislocations are efficient precipitation sites for copper. Therefore, this result gives us reasons to believe that electrostatic effects are also involved in precipitation of copper at extended defects associated with oxygen precipitates.

Presently, we can suggest the following model: as long as Fermi level in the sample lies above the energy level of dislocations, punched out by the oxygen precipitates, these dislocations (which are thought to form acceptor levels in the band gap) are negatively charged and attract positively charged interstitial copper ions. If the Fermi level drops below the energy level of these dislocations in the band gap, they change their sign from negative to neutral or positive, and copper precipitation slows down considerably. This hypothesis is similar to our model of Fermi-level dependent precipitation behavior of copper in the bulk of FZ wafers [7], based on our finding that copper-silicide precipitates, which form in the bulk of silicon after a rapid quench, form a defect band located in the upper half of the band gap between $E_C - 0.15 \text{ eV}$ and $E_C - 0.35 \text{ eV}$ [6]. The copper-silicide precipitates were shown to be amphoteric and change their charge state from positive to negative as the Fermi level goes upwards and crosses the electroneutrality level of the precipitates at approximately $E_C - 0.2 \text{ eV}$. Coulomb repulsion between the positively charged Cu_i^+ ions hinders clustering of copper, and repulsion between the growing Cu precipitates and Cu_i^+ greatly decreases bulk precipitation rate in FZ silicon, unless the Fermi level lies sufficiently close to the conduction band edge. This can be achieved either in sufficiently doped *n-Si* samples, or in *p-type* samples with sufficiently high density of Cu_i^+ , which inverts the conductivity type of the sample. We suggested that since electrostatic repulsion prevents growth of copper precipitates in the bulk, most of the copper diffuses out in *p-Si*, unless the starting copper concentration is high enough to change the charge state of copper precipitates (see [7] for more details). The effect of outdiffusion of copper to the wafer surfaces was demonstrated experimentally by Shabani *et al.* [8] and McCarthy *et al.* [9].

An experiment similar to those described above and presented in Figs. 1 was performed using EFG multicrystalline material. As it follows from Fig. 2, 90% of the copper has precipitated in the bulk. However, the remaining 10 percent did not precipitate and could be detected as interstitial copper by TID 30 min after the quench. The kinetics of decay of the residual copper concentration, monitored by TID over the subsequent 24 hours, was in a good agreement with the model of outdiffusion of copper to the wafer surface without any precipitation in the bulk. This result is similar to that obtained on Si10 and Si11 CZ samples.

Thus, the following conclusions can be made. First, EFG silicon provides very high density of precipitation sites for copper in the bulk of the wafer, comparable to the density of precipitation sites in CZ silicon with 10^{10} to 10^{11} cm⁻³ of oxygen precipitates in the bulk. However, these precipitation sites do not getter all the copper. In fact, almost 2×10^{14} cm⁻³ of copper remains ungettered 30 min after the quench, although the precipitation rate predicted by Hams law for as high density of defects as it is available in the EFG material would be sufficient for all copper to precipitate within several minutes or less. This residual copper may diffuse to the *p-n* junction and form precipitates there, which may eventually decrease open-circuit voltage of even form shunts.

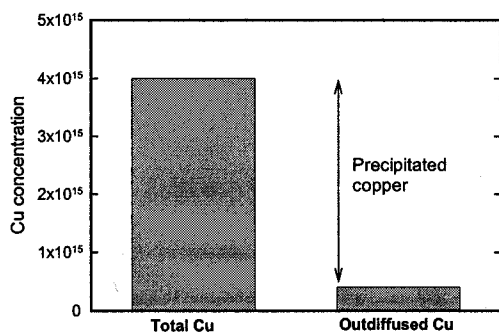


Fig. 2. Result of a TID measurement on EFG material. While most of copper has precipitated, non-negligible fraction of it remains in the bulk even 30 min after the quench. The residual copper concentration is similar to that observed in CZ samples.

Our data, presented in this report, suggest that electrostatic effects, which we proposed to explain these observations, are as much important in the EFG material as they are in CZ silicon with oxygen precipitates. Understanding these effects is important to the description of the physics of copper in multicrystalline silicon for solar cells. Detailed studies of the role of electrostatic effects on copper precipitation at extended

defects in silicon are in progress and will be reported elsewhere.

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CHARACTERIZATION OF CZOCHRALSKI SOLAR CELLS GROWN WITH A RECHARGE PROCESS

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Abstract

Siemens Solar Industries (SSI), in cooperation with the Northwest Energy Efficiency Alliance (NEEA), has developed a multiple batch recharge system. The multiple batch recharge Czochralski process dramatically reduces costs, energy consumption, material handling, and labor while increasing yields, throughput, and process capabilities. Data will show the levels of metals, Carbon, and Oxygen in ten sequential ingot sections grown at SSI. Solar cells and modules manufactured from recharge ingots show consistent performance with those grown from standard batch processes.

Introduction

In April of 1998, Siemens Solar Industries entered into a jointly funded project with the NEEA to develop a more energy efficient approach to crystal growing. The established project objectives were very ambitious:

Goals	Achievements
1)Reduce power consumption by 40% per run (kwh/kg)	1)Reduced power consumption by 51% per run (kwh/kg)
2)Reduce Argon consumption by 50% per run (cf/kg)	2)Reduced Argon consumption by 85% per run (cf/kg)
3)Increase productivity by 15% (mm/day)	3)Increased productivity by 35% (mm/day)
4)Improve or maintain the quality of the ingot produced	4) 5% higher valued solar cells -better axial Oi
5)Transform the market place, specifically semi-conductor crystal growers in the Northwest, into lower consumers of power and Argon.	5)Agreement with Wacker and in discussions with MSA. • 30% lower ingot costs • 15% higher yields

Under the scope of the project, SSI's hotzones were extensively modified with an energy efficient hotzone (EEH) to meet the technical goals shown above. However, the addition of insulation resulted in a 20% reduction of the initial charge capacity.ⁱ Therefore, SSI developed a system to add material to the crucible during meltdown. The system was called a topping off system. With the topping off system in place it was also possible to develop a recharge or semi-continuous process. In addition, a market analysis of the Northwest semiconductor manufacturers, engineers, and managers showed much of the interest in the project focused on recharge technology.ⁱⁱ With that in mind, SSI shifted its efforts from topping off the initial charge to refining multiple batch recharge. The achievements, shown above, have been demonstrated for systems with an improved hotzone and recharge process.

Results and Discussion

Ingots grown from standard and recharge systems were collected to characterize ingot quality and cell performance. Three tests were completed. For the first and second test, samples from the top (seed end) and the bottom (tang end) of ten consecutive recharge ingots were used. Samples were sent to independent companies for analysis. The ingot analysis consisted of glow discharge mass spectrometry (GDMS) for metal content and fourier transform infrared spectroscopy (FTIR) analysis for carbon and oxygen content. The third test used a random selection of recharge ingots to compare cell and module performance against standard (non-recharge) material.

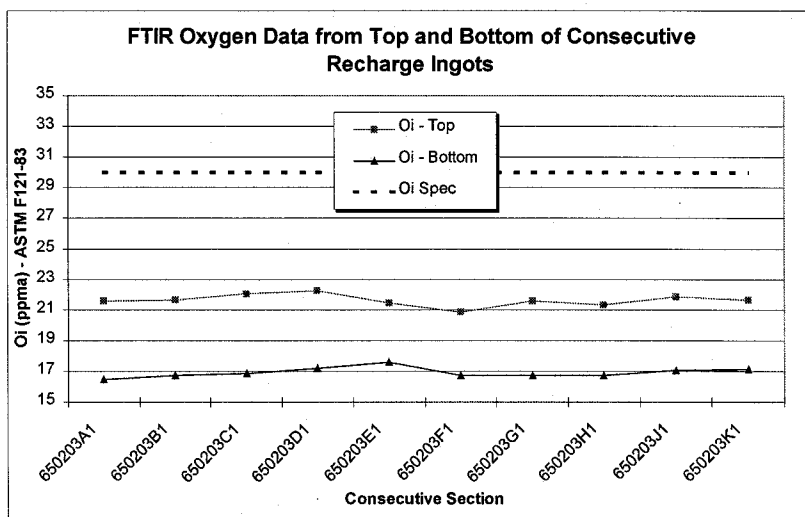
1. GDMS Analysis

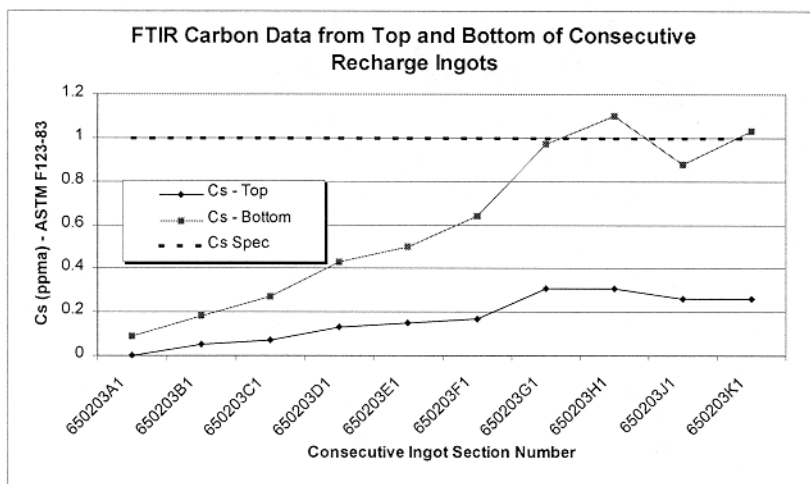
The GDMS is capable of detecting trace levels, (> 5 ppb) and in some cases (> 2 ppb), of metallic contaminants. Samples were cut, rinsed, and labeled before shipping. The laboratory etched the wafers and conducted the tests. The GDMS analysis looked for detectable levels of Fe, Cr, Mo, Al, Ni, and Ba. These metals were selected because of their segregation levels and detriment to the ingot's electrical characteristics. Segregation would suggest the highest level of impurities would be found in the bottom of the last ingot section analyzed. The investigation of all recharge samples with GDMS showed the accumulation of impurities did not reach the detection limits for any of the metals.

2. FTIR Analysis

The FTIR analysis examined axial Oxygen and Carbon content in the ingot. Again, samples from the top and bottom of the same 10 recharge ingots were examined. The samples were chemically polished until a mirror smooth surface was obtained. The samples were analyzed using a Bio-Rad QS-300. The data gathered for interstitial oxygen, Oi, was correlated to SRM 2551. All data reported for Oi is in ASTM F121-83 units. All data reported for Cs is in ASTM F123-83 units. The machine was monitored hourly to insure the stability of the readings. Each slug was measured at the center point for Oi and Cs.

The FTIR Oxygen chart shows that Oi content is consistent from ingot to ingot. Ingots are grown from the same crucible and are all 145 mm diameter ingots greater than 800 mm in length. The i-th section was a short section and was not used in the analysis. This recharge run lasted over 200 hours.

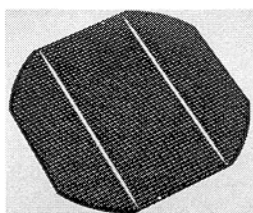




The FTIR chart for Carbon shows an increasing level of Cs. Carbon is abundant in the hotzone. It is the primary constituent of the graphite components that make up the EEH. At the high temperatures the machines operate, CO and CO₂ are readily produced and can be incorporated in the

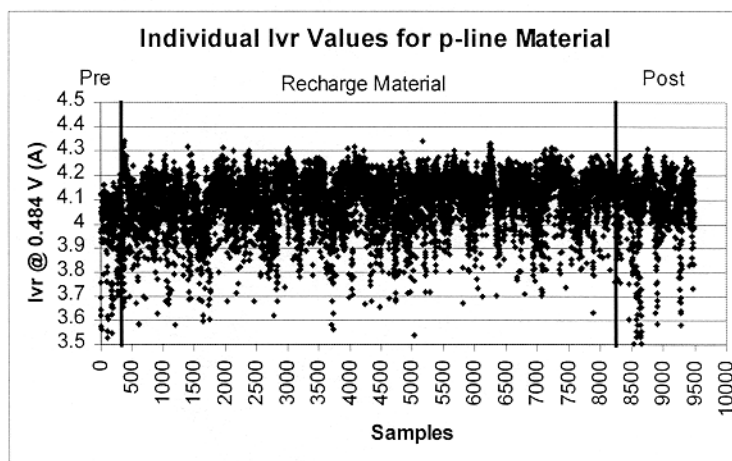
melt. However, the largest source of Carbon originates from the starting polycrystalline materials.ⁱⁱⁱ In solar products Carbon content can vary because a great portion of the starting materials are recycled and are not characterized. As a result, the Carbon content in the ingot can vary. In this case, the recharge ingots show a steady increase consistent with the segregation of Carbon and the addition of new Carbon from recharge material.

3. Solar Cell Characterization

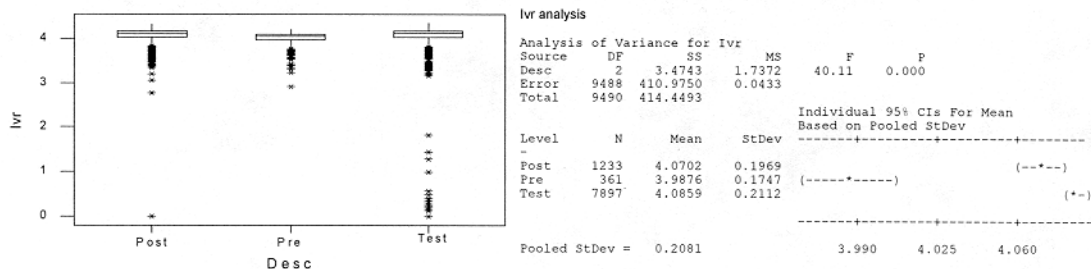


Samples grown from randomly selected recharge sections were processed into p-line solar cells, shown left, using the SSI manufacturing facility in Camarillo, California. A total of 11 recharge sections were processed into 315 micron wafers and subsequently solar cells. The 11 sections included material from the first, middle, and ends of recharge runs. A batch of

approximately 7500 wafers (Test) were compared to cells prior (Pre) to the experiment and after the experiment (Post). The cells processed before and after the experiment were from ingots grown in the standard batch process. A chart of current at a rated voltage (I_{vr}) shows the consecutive cell results from Pre, Test, and Post solar cells.

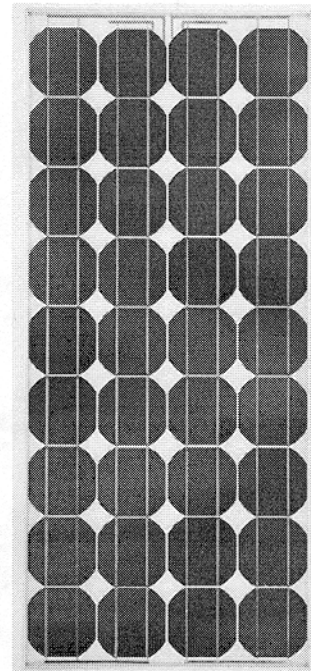
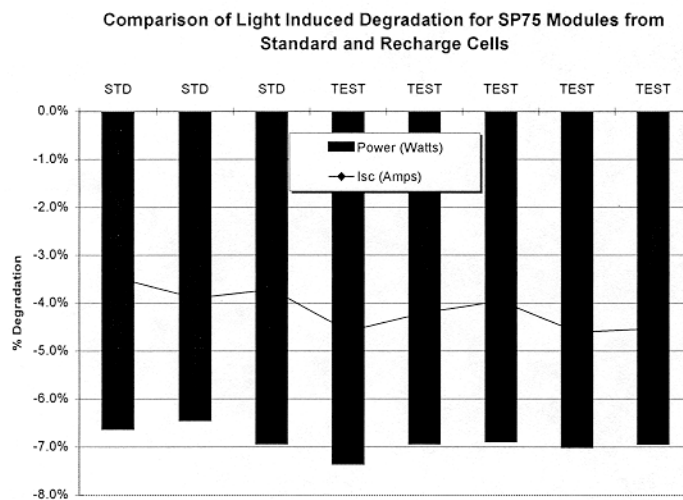


A one way ANOVA and box and whiskers analysis of the data shows only a slight statistical difference between all of the electrical characteristics studied., including I_{sc}, V_{oc}, FF, and I_{vr}.^{iv} An example of the I_{vr} analysis is shown. The difference in electrical characteristics between standard and recharge materials is small. Therefore, the recharge



process yields material capable of making effective solar cells and is consistent with SSI's standard processed material.

The cells were then assembled into SP75 modules and tested for light induced degradation (LID). Degradation would be expected if excessive metallic impurities were accumulating in the subsequent recharge sections. While the tests show a slightly higher level of degradation for power and Isc, the test modules performed consistently with one another. Again, the affects of recharging on LID are comparable with standard ingots.



Conclusion

The ingot, cell, and module results show that material grown from recharge systems can perform as well as material grown from standard or non-recharge processes. The economic benefits of using the recharge process are enormous in that yields and productivity improve, while lowering cost, materials, and energy consumption. The authors thank the Northwest Energy Efficiency Alliance (NEEA) for their continued support, without which this publication and the realized benefits would not have been possible.

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ⁱⁱ John Reed, Andrew Oh, and Nicholas Hall in: Market Progress Evaluation Report: Silicon Crystal Growing Facilities, No. 1 – Report #E99-034, NEEA, August, 1999.

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^{iv} D. Montgomery, Design and Analysis of Experiments, pp. 67-79. John Wiley & Sons, New York, 1997.

Characterization of the Gettering and Anti-Reflective Properties of Ti Thin Films

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ABSTRACT: Ti, TiN_x, TiN_xO_y, TiO_x, TiC_x and TiN_xC_y films were deposited using magnetron sputtering on Fe Contaminated Silicon Wafers. After film deposition, the wafers were annealed in a nitrogen/oxygen atmosphere at 700°C (150min) in order to getter metal impurities. The optical, surface, and chemical characterizations were carried out for annealed and reference wafers. Low reflectance, good surface quality, and excellent temperature stability have been found for TiO_x and TiN_xO_y films.

1. Introduction

Titanium oxide films are used in a wide range of applications. Its high refractive index, wide bandgap and chemical stability make them suitable for photo-voltaic applications as a photo-electrode in solar cells, catalytic surfaces and antireflective coating [1]. Titanium nitride films are used as contact layers for solar cells, diffusion barriers and Schottky contacts in microelectronics. They are also wear-resistant surfaces [2] with an excellent high temperature stability. Recently it was shown that Ti_{1-x}Si_xN_y thin layer prepared by magnetron sputtering is also a good wear-resistant film [3]; whereas TiC_x is a hard material coating not generally used in PV technology. We expect that C atoms can modify interface surfaces during getter annealing and change its getter properties. Recently, we have shown that a Ti film can be used as an external getter, and that simultaneously during formation of the Ti nitride in argon-nitride plasma, vacancies are injected into the Si bulk during annealing at 700°C [4]. We previously reported [5] lifetime improvement for Ti film getter, which was comparable to Al getter efficiency. In this paper we report on the optical properties of the Ti, Ti oxide, Ti nitride, and Ti carbide films following annealing. The gettering ability of the above films will be described in a separate paper. The long-term temperature treatment used for external gettering can modify optical properties of the film, because of surface reconstruction, new phase formation and evaporation.

2. Experiment

Film Preparation

The films were prepared by pulsed magnetron sputtering onto Si 100 substrate at room temperature. P-type Si wafers were intentionally contaminated with iron to a concentration of $\sim 5 \times 10^{12} \text{ cm}^{-3}$. Prior to deposition, JTB cleaning was carried out for 5 min at 75°C following a 5 min rinse in DI water, 10 sec in an HF water solution (1:10), and final rinse in DI water for 5 min. Seven Ti films were deposited in a 2mTorr Ar plasma containing diluted gasses of 0.2 mTorr each: (1) pure Ar plasma, (2) Ar & N₂ plasma, (3) Ar & N₂ & O₂ plasma, (4) Ar & O₂ plasma, (5) Ar & O₂ plasma-150°C, (6) Ar & CH₄ plasma, (7) Ar & CH₄ & N₂ plasma. The initial vacuum was 5×10^{-6} Torr and the Ti target was pre-cleaned in Ar plasma for 3min. The films were deposited for 15 min with a target current of 0.3A and the film thickness about 35 nm. The gettering-annealing process was performed in nitrogen and oxygen gas flows of 720sccm and 720sccm, respectively at 700°C for 150min. Films were examined by AFM, XRD, and optical reflectometer before and after annealing.

Atomic Force Microscopy The film surface measurements were carried out using an AFM D-3000 in tapping-contact mode with a silicon cantilever probe in ambient air covering 1 x 1 and 5

$\times 5 \mu\text{m}^2$ scanning areas. For each case the rms-roughness was evaluated. The rms data are presented in Table I. The minimum roughness obtains for TiN_xO_y and the maximum for a TiC_x film. The roughness of the TiO_x film deposited at room temperature (RT) and at 150°C is low at $\sim 0.19 \text{ nm}$. Note that having N_2 gas added to the plasma, diminishes surface roughness, compare TiO_x , TiN_xO_y and TiC_x , TiN_xC_y in Table I. 3D AFM images of the films, see Fig.1, show that the Ti film surface roughness is larger than for TiN_xC_y , TiN_xO_y , and TiO_x . Figure 2 shows 2D AFM images of the four samples of Fig. 1 after getter/annealing. The grain size is larger than before annealing. Note that unique “worm-like” patterns are formed for TiN_xO_y and TiO_x samples deposited at RT, while the patterns are not seen for the TiO_x sample deposited at 150°C .

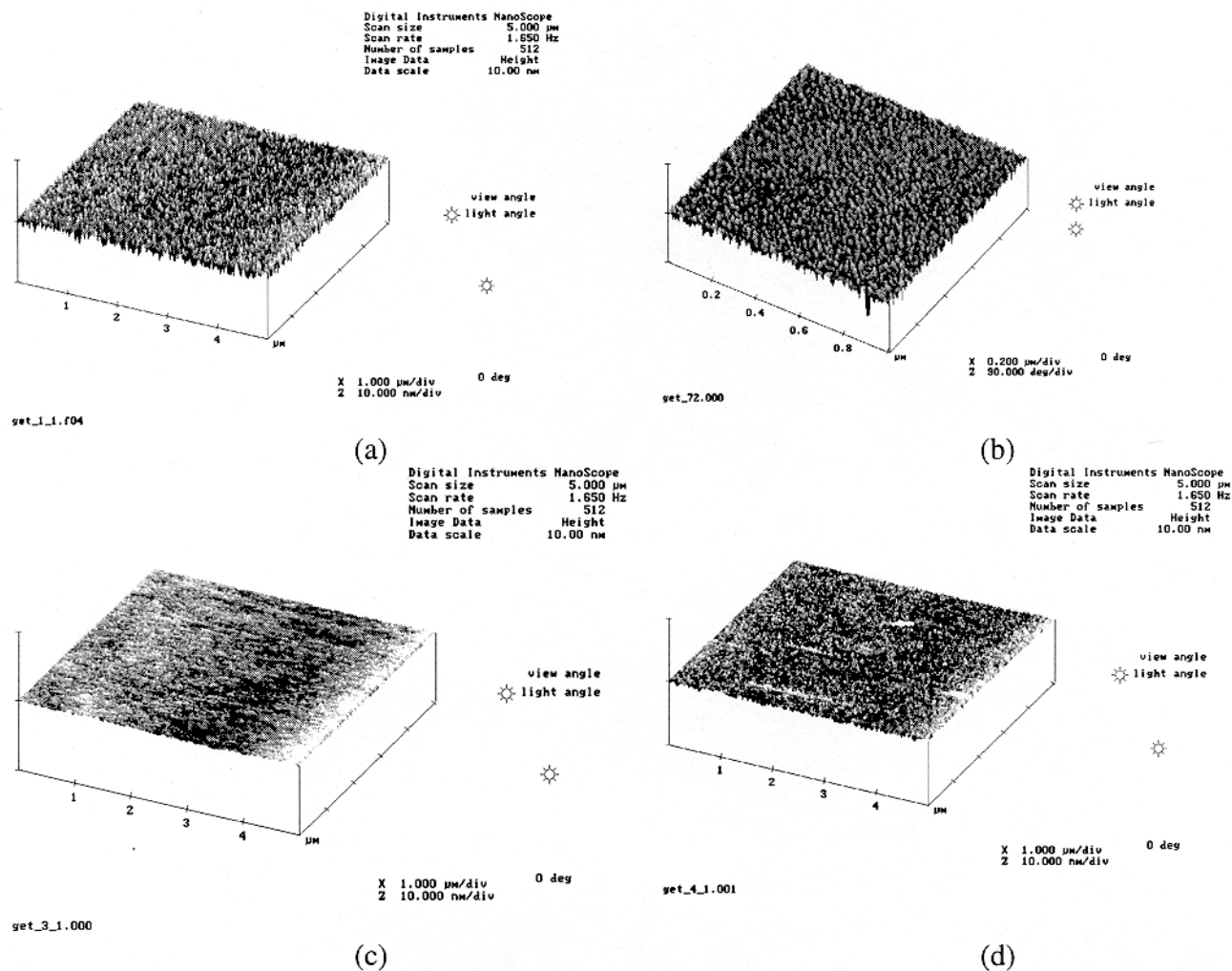


Fig. 1. 3D AFM images of non-annealed Ti thin films deposited by magnetron sputtering with different plasma gases, (a) Ti/Ar; (b) $\text{TiN}_x\text{C}_y/\text{Ar}$ & N_2 , CH_4 ; (c) $\text{TiN}_x\text{O}_y/\text{Ar}$ & N_2 , O_2 ; (d) TiO_x/Ar & O_2 .

X Ray Diffraction XRD measurements were made in the Bragg-Bretano arrangement. Of the three films measured (TiN_xO_y , TiO_x and TiC_x) TiO_2 peaks were only recognized for the first two films before annealing, while after annealing most of these lines were diminished. The XRD lines observed for TiC_x disappeared after annealing, indicating low stability or low adhesiveness.

Optical Characterization The model F20-UV thin film optical system manufactured by

Filmetrics, Inc. has been used for measuring wafer reflectance. The reflectance spectra were measured from 224 to 845 nm. Because of a low film thickness of $\sim 30\text{nm}$, the standard software

Table I

Film	rms-roughness [nm]						
	Ti RT	TiN _x RT	TiN _x O _y RT	TiO _x RT	TiO _x 150 ⁰ C	TiC _x RT	TiN _x C _y RT
Non-gett	0.47	0.49	0.15	0.19	0.19	0.83	0.36
Gettered	6.01	10.32	1.53	1.47	13.52	7.80	7.53

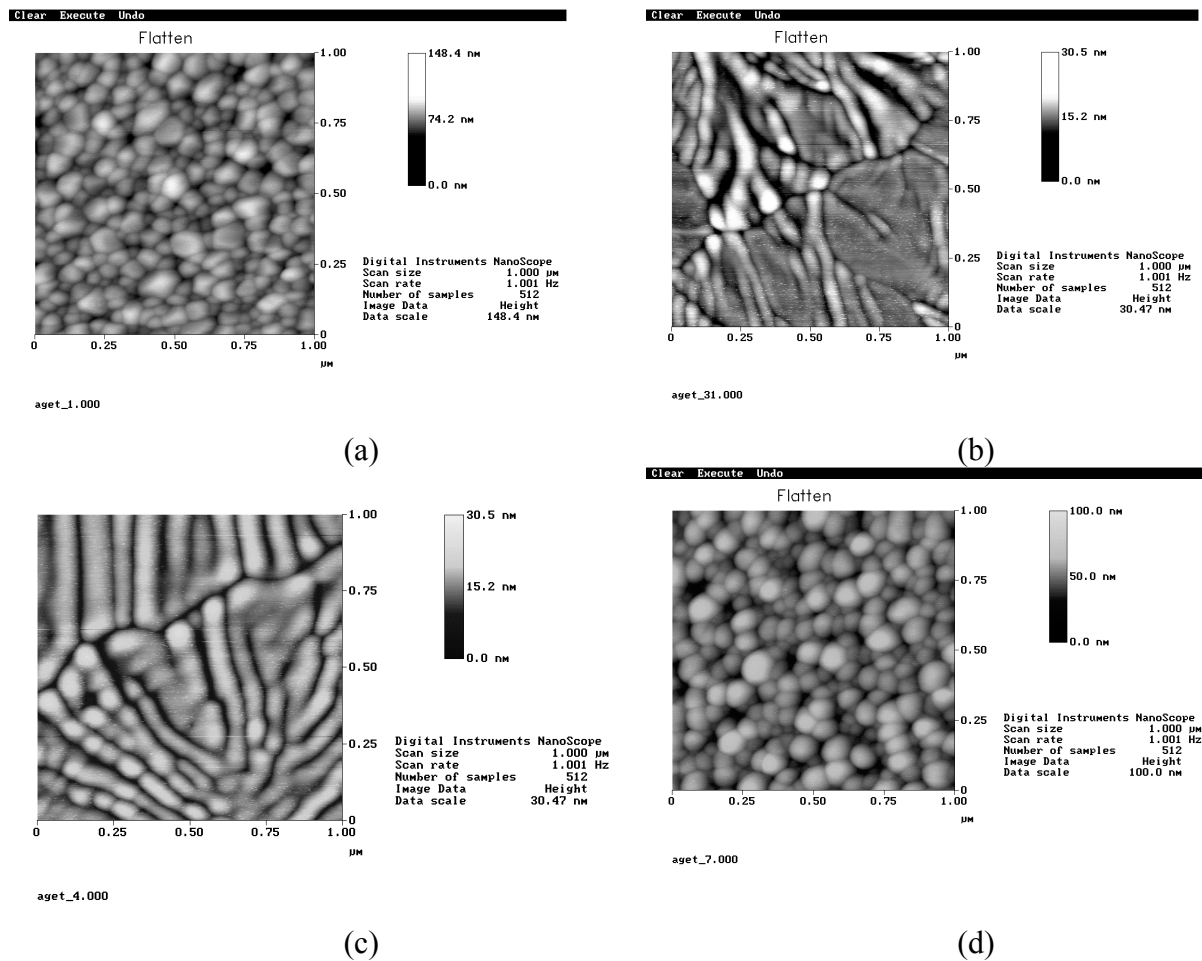


Fig. 2. 2D AFM image of annealed Ti films, (a) Ti film, (b) TiN_xO_y film, (c) TiO_x film, and TiN_xC_y film.

could not be used for refractive index and extinction coefficient evaluation. The reflectances of the non-annealed samples are presented in Fig. 3a. A long-wavelength reflectivity of 0.3 is seen for Si, TiN_xO_y, and TiO_x films. In the case of Ti, TiO-1500C, TiC and TiN_xC_y films, the reflectance increases with wavelength and reaches a value of about 0.6 for Ti film due to the presence of metal atoms. Metal domination is also seen for TiO_x deposited at 150⁰C. After

annealing, more of the spectra change, as shown in Fig. 3b. Only the TiN_xO_y and TiO_x film spectra remained the same. In the modeling of the reflectance spectra, the Drude-Lorentz (D-L) oscillator model [6] was implemented. This model matches well the whole wavelength range spectra of Ti and TiN_xO_y . Both curves differ with damping parameter γ and high frequency dielectric function ϵ_∞ , indicating metallic domination in the first case and silicon domination in the second.

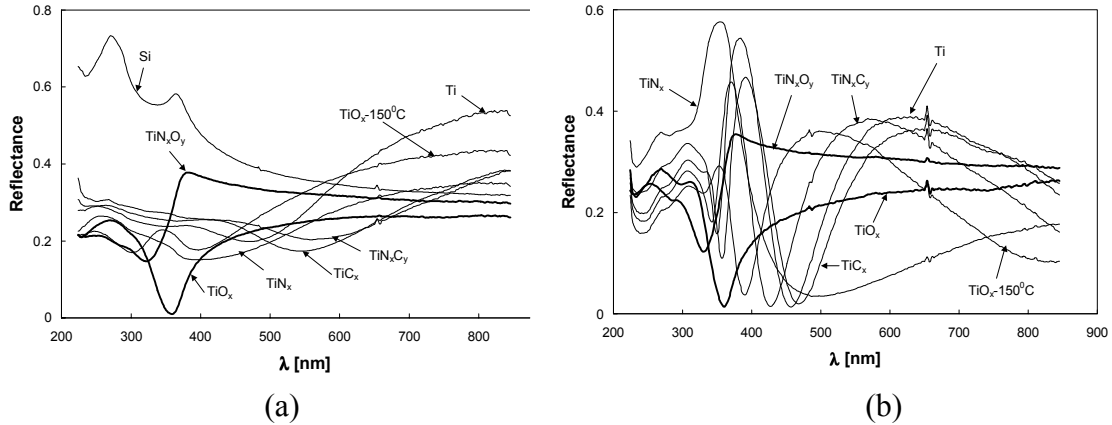


Fig. 3. The reflectance of non-annealed (a) and annealed (b) wafers.

The D-L model could not match the non-annealed TiO_x and non-annealed Ti spectra. In this case the dielectric function (DF) was obtained by a combination of the single-layer Fresnel's and Forouhi Bloomer (FB) equations [1]. Good agreement has been reached in the short wavelength part of the spectrum. The long wavelength part of the TiO_x spectrum has been simulated using Fresnel's and D-L equations.

3. Discussion and Conclusions

TiO_x and TiN_xO_y are temperature resistant and can be used as external getters. TiN_xC_y , and TiC, and Ti films become less metallic after annealing. Low reflectance, below 0.3, is due to surface roughens, which has been confirmed by the AFM study. The high frequency dielectric function of a TiN_xO_y film of 14.5 is almost equal to the silicon ϵ_∞ , indicating film transparency at the long wavelength range. The fitted E_{FB} energy of 2.15eV for TiO_x film agrees with literature data for crystalline Ti oxide [1]. A lifetime data and iron concentration measured using DLTS after getter/annealing we will present on the Poster Session.

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Understanding and optimization of Al-enhanced SiN_x induced defect passivation in ribbon silicon

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Abstract

Hydrogen passivation of defects in ribbon silicon materials via the post-deposition anneal of PECVD SiN_x films increases substantially in the presence of an Al layer. A three-step physical model has been proposed to explain the defect passivation due to a positive synergistic effect during the simultaneous anneal of a PECVD SiN_x film on the front and a screen-printed Al layer on the back. According to this model, defect passivation is governed by the release of hydrogen from the SiN_x film, the generation of vacancies during Al/Si alloying, and the retention of hydrogen at defect sites in silicon. RTP and belt furnace anneal temperatures were optimized for maximum defect passivation in EFG and String Ribbon silicon respectively, and found to be in the range of 825°C – 850° C for 2 minute anneals. Corresponding devices fabricated on String Ribbon silicon also show a 0.5% (absolute) higher efficiency when the anneal temperature is 850°C. Controlled rapid cooling for improved hydrogen retention was found to increase the SiN_x induced defect passivation in String Ribbon silicon substrates and has resulted in large area EFG cell efficiencies of 14.7%.

Introduction

Ribbon silicon growth technologies are attractive for silicon photovoltaics because thin (~100 μm) substrates can be grown directly from the melt, eliminating the losses associated with wafer slicing and etching. However, the performance of ribbon silicon solar cells is limited by the bulk minority carrier lifetime, which is typically in the range of 1-10 μs in the as-grown state. Model calculations reveal that for high efficiency (~16%), thin screen-printed devices, the bulk lifetime must be improved to greater than 20 μs, the rear surface recombination velocity reduced to 100 cm/s, and the fill factor improved to 0.77.

The purpose of this work is to optimize the simultaneous SiN_x/Al anneal temperature for defect gettering and passivation in an effort to improve the basic understanding of SiN_x induced hydrogen passivation of defects in silicon. The temperatures of RTP and belt furnace anneals of SiN_x/Si/Al are optimized for gettering and passivation through minority carrier lifetime measurements on 3 -cm EFG and

String Ribbon silicon substrates. Corresponding solar cells are fabricated on String Ribbon silicon to demonstrate the impact of the optimum anneal temperature on device performance. In addition, the impact of controlled rapid cooling for improved hydrogen retention and defect passivation is investigated on String Ribbon substrates and large-area screen-printed EFG cells.

Experimental

Lifetime measurements were made by the quasi-steady state photoconductance (QSSPC) technique [1] with samples immersed in an I_2 /methanol solution that has been shown to effectively passivate Si surfaces [2]. Lifetime values were recorded at an injection level of $1 \times 10^{15} \text{ cm}^{-3}$ to avoid recording erroneously high recombination lifetimes at lower injection levels caused by shallow traps [1]. After the initial lifetime measurement, substrates were cleaned and subjected to aluminum gettering and SiN_x -induced hydrogenation individually or in combination with the appropriate heat treatments performed in a belt furnace or an RTP system.

Results and Discussion

Optimization of the simultaneous SiN_x/Al anneal temperature in an RTP system for defect gettering and passivation

The results of SiN_x induced defect passivation and Al gettering in EFG silicon, individually and in combination, as a function of the RTP anneal temperature are shown in Figure 1. The as-grown

lifetime of EFG wafers in this study was in the range of 1.5-2.0 μs . SiN_x induced defect passivation was ineffective at temperatures below 600°C, but improves the bulk lifetime by about 1 μs when the anneal temperature was raised to 700°C. FTIR measurements of annealed PECVD SiN_x films have shown that the release of hydrogen from the SiN_x film is low at low temperatures [3]. We propose a three step

physical model according to which defect passivation is governed by the release of hydrogen from the SiN_x film, the generation of vacancies, and the retention of hydrogen at defect sites in silicon. In accordance with this model, at low temperatures ($<700^\circ\text{C}$), defect passivation is limited by the release of hydrogen from the SiN_x film. When the anneal temperature is high ($>800^\circ\text{C}$), Figure 1 shows that no improvement in the bulk lifetime is observed even though the release of hydrogen from the SiN_x film is high,

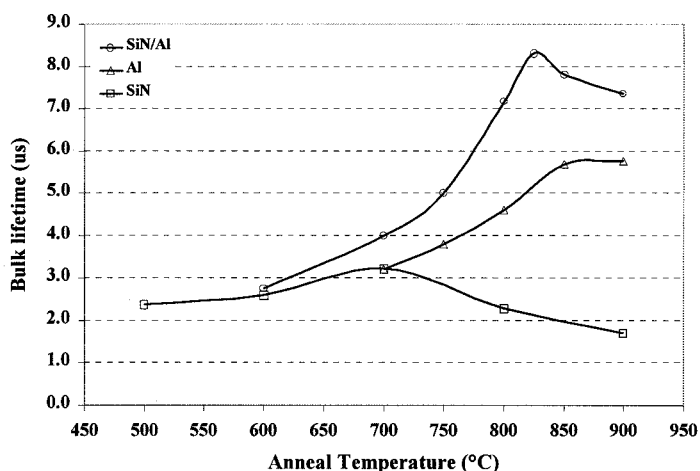


Figure 1: Optimization of RTP Al gettering and SiN_x induced defect passivation in EFG silicon

because the retention of hydrogen at defect sites in silicon is low. It is well known that hydrogen can evolve out of silicon at temperatures above 500°C during prolonged anneals [4]. The competition between the release of hydrogen from the SiN_x film and the retention of hydrogen at defect sites in silicon results in an optimum anneal temperature at 700°C for the SiN_x induced passivation of defects in EFG silicon. The effectiveness of Al gettering of EFG silicon increases with anneal temperature, as shown in Figure 1, resulting in a bulk lifetime of about 5 μs at 850°C - 900°C. The effectiveness of Al gettering of transition metals is expected to increase with the anneal temperature because of their higher diffusivity in silicon and solubility in the aluminum melt at high temperatures.

The combined effect of simultaneous SiN_x induced defect passivation and Al gettering (Al/SiN_x) in EFG silicon is shown in Figure 1. Like the SiN_x induced defect passivation of EFG, an optimum RTP anneal temperature exists for the simultaneous Al and SiN_x anneal as a result of the competition between the release of hydrogen from the SiN_x film and the retention of hydrogen at defect sites in silicon. However, the presence of Al on the back of the wafers during the anneal shifts of the optimum anneal temperature to 825°C and increases the maximum lifetime to 8 μs as shown in Figure 1. This improvement in lifetime is much greater than the sum of the improvements due to the individual SiN_x and Al treatments for all temperatures in Figure 1 above 700°C, indicating that there is a synergistic interaction between the hydrogenation process and Al/Si alloying above 700°C. According to our model, vacancies, generated in silicon during Al/Si alloying, increase the dissociation of molecular hydrogen into atomic hydrogen [5] and enhance the transport of hydrogen in silicon. The binding energy of hydrogen to vacancy clusters [6] provides an additional driving force for the diffusion of hydrogen enabling the passivation of defects deep in silicon. At low temperatures, the effect of the SiN_x /Al anneal is limited by the release of hydrogen from the SiN_x film, as well as the low generation of vacancies during Al alloying, and the ineffectiveness of Al gettering. At temperatures just above the melting point of Al ($T_m=660^\circ\text{C}$), the number of vacancies generated in Si during Al/Si alloying is believed to be low, as the equilibrium solubility of Si in the Al melt is low ($X_{\text{Si}} \sim 16\text{-}17\%$ at.). Few vacancies are available to participate in the dissociation of molecular hydrogen into atomic hydrogen. Thus at low alloying temperatures, the concentration of atomic hydrogen and the driving force for its diffusion are expected to be low. As the temperature increases to 700°C, the release of hydrogen from SiN_x is increased, but vacancy generation is still low due to the low solubility of Si in the Al melt ($X_{\text{Si}} \sim 20\%$ at.) and, as shown in Figure 2, there is no synergistic effect. As the equilibrium solubility of Si in Al increases to about 30 % at. at 825°C, the number of vacancies generated at the Al/Si interface increases significantly. Thus the SiN_x induced defect passivation is enhanced by vacancies generated during Al alloying at high temperatures, which increase dissociation of molecular hydrogen and diffusion of atomic hydrogen. The absolute lifetime values shown in Figure 1 are low due to the absence of prior phosphorus gettering.

Optimization of the simultaneous SiN_x /Al anneal temperature in a belt furnace for defect gettering and passivation

Figure 2 shows the variation of the effectiveness of the Al-enhanced SiN_x induced hydrogenation of defects in String Ribbon silicon with simultaneous anneal temperature in a belt furnace. The average as-grown lifetime of each sample in Figure 2 was in the range of 13.4 to 13.6 μs . The results in Figure 2 indicate an optimum anneal temperature for bulk passivation exists at 825°C. The simultaneous process becomes detrimental to the bulk lifetime when the anneal temperature is 900°C. The dramatic decrease in the defect passivation at 900°C may be the result of a decreased retention probability of hydrogen at defects in silicon at high temperatures. Additionally, it has been shown that screen-printed Al paste, in which iron is a contaminant, when annealed at high temperatures, can inject harmful impurities to the back of mc-Si wafers, reducing the bulk lifetime in the device [7].

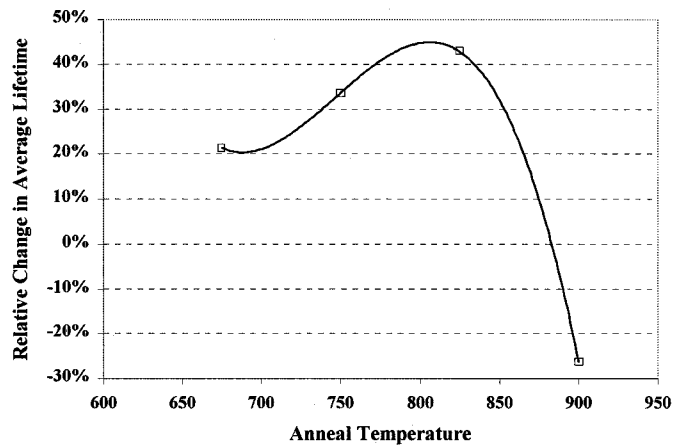


Figure 2: Optimization of the belt furnace Al/ SiN_x anneal temperature for bulk gettering and passivation in String Ribbon silicon.

Impact of the simultaneous Al/ SiN_x anneal temperature on String Ribbon solar cell performance

To study the effect of the simultaneous anneal temperature on String Ribbon solar cells, devices were fabricated with the Al/ SiN_x anneal temperature in the range of 650-950°C. The fabrication process included emitter diffusion in a belt furnace to achieve a sheet resistance of 45 Ω/\square followed by PECVD SiN_x deposition onto the front surface of all samples. After Al screen-printing onto the back surface, samples were annealed in a

belt furnace at a temperature of 650°C, 850°C, or 950°C. Front grid metallization was formed by evaporation and liftoff photolithography. The average performance of the cells is shown in Table 1 and plotted with the simultaneous anneal temperature in Figure 3 along with the average as-grown lifetime of each wafer. The cells fabricated with the

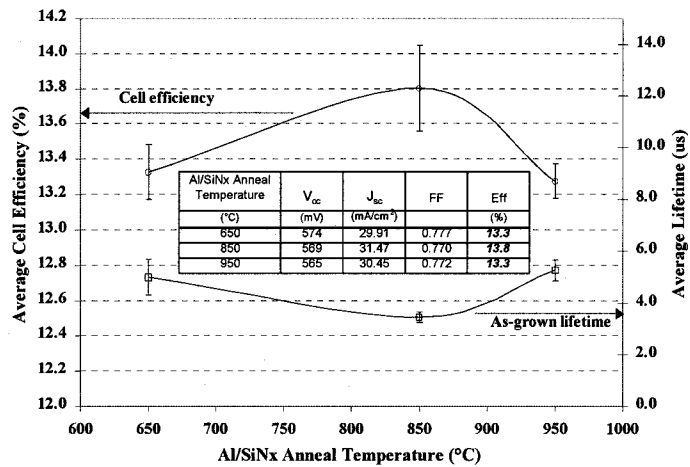


Figure 3: Impact of the Al/ SiN_x belt furnace anneal temperature on the performance of String Ribbon silicon solar cells

simultaneous anneal performed at 850°C showed a 0.5% (absolute) higher efficiency than those fabricated with the simultaneous anneal performed at 650°C or 950°C. This efficiency difference is attributed to different bulk lifetimes in the cells because it is mostly reflected in the difference in J_{sc} . This hypothesis is supported by LBIC analysis of selected devices that indicates defect passivation was most effective during the 850°C anneal. Screen-printed String Ribbon silicon solar cells have also been fabricated with the SiN_x/Al anneal performed at 850°C with efficiencies as high as 14.6%.

Controlled rapid cooling for improved SiN_x induced defect passivation

Controlled rapid cooling was investigated to improve the retention of hydrogen at defect sites in String Ribbon silicon substrates. After SiN_x deposition onto both surfaces, samples were annealed at 850°C for 2 minutes and cooled to 500°C at controlled rates of -5°C/s to -44°C/s followed by rapid cooling to room temperature.

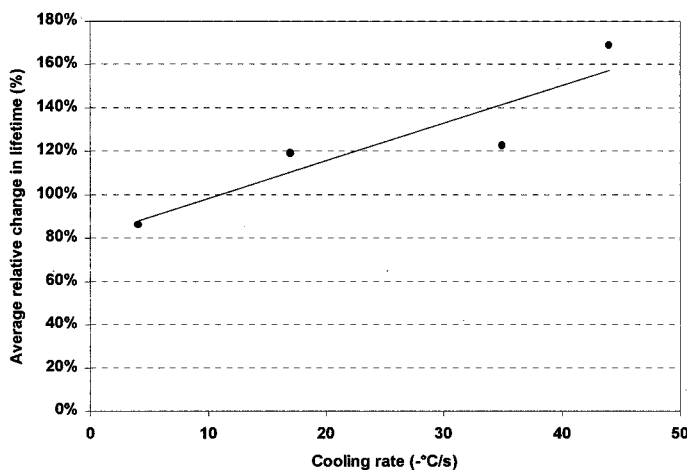


Figure 4: Effect of controlled rapid cooling on the SiN_x induced passivation of defects in String Ribbon silicon

Figure 4 shows that the relative improvement in lifetime increases as the cooling rate after the 850°C SiN_x anneal increases. This result suggests that the retention of hydrogen at defect sites in silicon can be improved by increasing the cooling rate after the anneal. When the cooling rate is low (-5°C/s), the improvement in lifetime is below 100%. When the cooling rate increases to -50°C/s , the improvement in lifetime increases dramatically to near 170% due to the higher retention of hydrogen at defect sites.

Effect of controlled rapid cooling after the co-firing of large area screen-printed EFG cells

To investigate the effect of controlled rapid cooling in the co-firing of screen-printed contacts, large area screen-printed EFG cells were fabricated. Emitter diffusion, SiN_x deposition, and the screen-printing of front and rear metallization were performed by ASE Americas. Cells were then co-fired in an RTP system with varying cooling rates. Figure 5 shows the effect of the post firing cooling rate ($A < B < C < D$) on the average cell performance of several 100 cm^2 EFG cells. The results clearly show that there is an increase in cell performance as the cooling rate is increased due to an increase in J_{sc} and V_{oc} with increasing cooling rate. While others have found that the cooling rate in the RTA cycle effects cell performance by influencing the contact resistance of screen-printed contacts [8], the results in Figures 4 and 5 indicate that the cooling rate effects the bulk lifetime of the material, increasing the J_{sc} and V_{oc} of the cells.

Conclusions

We have shown through minority carrier lifetime measurements on EFG substrates that an optimum SiN_x anneal temperature in an RTP system exists for bulk passivation. It is believed that the optimum is a result of the competition between the release of hydrogen from SiN_x film and the retention of hydrogen at defect sites in silicon. The simultaneous RTP anneal of the SiN_x film on the front and

a screen-printed Al layer on the back of EFG wafers increases the optimum anneal temperature to 825°C and increases the bulk lifetime to $8\ \mu\text{s}$. Lifetime measurements and solar cells fabricated on String Ribbon silicon substrates indicate that an optimum belt furnace SiN_x/Al anneal temperature exists in the range of 825°C - 850°C . Controlled rapid cooling was found to improve the retention of hydrogen at defects in String Ribbon silicon substrates during SiN_x induced defect passivation. The co-firing of EFG silicon with controlled rapid cooling resulted in $100\ \text{cm}^2$ cell efficiencies as high as 14.7%.

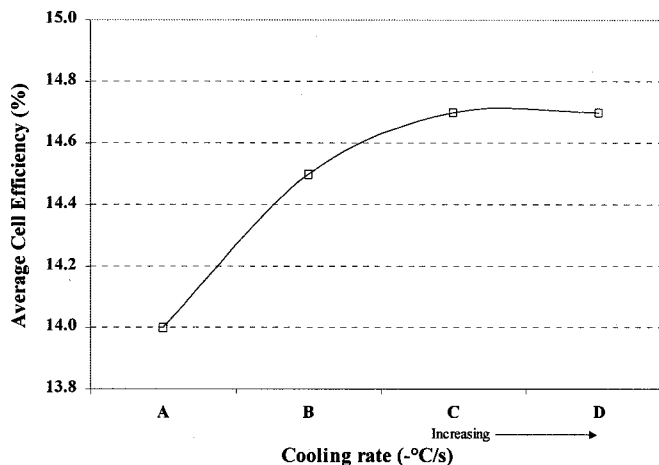


Figure 5: Effect of cooling rate on the performance of $100\ \text{cm}^2$ EFG silicon solar cells

Acknowledgements

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Belt Furnace Gettering and Passivation of n-Web Silicon for High Efficiency Screen-Printed Front Surface Field Solar Cells

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Abstract

Six different resistivities (0.32, 0.57, 1.2, 2.2, 9.1 and 20 Ω -cm) were investigated to understand the dopant-defect interaction in n-type, antimony doped, dendritic web silicon ribbon and study its response to gettering and passivation during belt furnace processing (BFP). The as grown lifetime was found to be a strong function of resistivity with higher resistivity displaying higher lifetime. P gettering at 925°C/6 min raised the as grown lifetime of ~ 1 μ s in 20 Ω -cm n-web to 5.4 μ s. A combination of phosphorus gettering followed by simultaneous Al gettering and SiN hydrogenation raised the 20 Ω -cm n-web lifetime to 78 μ s. Unlike the as grown web, the processed lifetime was greater than 75 μ s for all resistivities with no clear doping dependence. This is attributed to the very effective gettering and passivation during the belt furnace processing. Front surface field (FSF) n^+ - n - p^+ cells were fabricated by spin-on phosphorus diffusion on the front and screen-printed Al on the back. A lifetime value of over 100 μ s was obtained in a 14.2% screen-printed FSF n-web solar cell fabricated on 100 μ m thick 20 Ω -cm substrate. The screen-printed FSF cell fabricated on (111) FZ gave an efficiency of 14.9% with a fill factor of 77.6%. These results are supported by model calculations, which revealed a maximum efficiency of $\sim 15\%$ for 100 μ m thick planar screen-printed FSF cells and their insensitivity to bulk lifetime above a 60 μ s value.

Introduction

Dendritic web is one of the most promising thin (100 μ m) silicon ribbon for solar cells. Dendritic web typically has no grain boundaries but it has multiple twin boundaries running parallel to the external surfaces [1,2]. These are located in a band about midway through the ribbon thickness. However, according to Cunningham et al. [3], most of the dislocations in as grown web silicon are electrically active, and accumulate near the twin boundaries forming a thin slab of highly defective material within the web ribbon. This is partly responsible for low as-grown lifetime in both p and n-type dendritic web silicon. Like in other defective materials the minority carrier lifetime in p-type dendritic web silicon is found to decrease with decreasing base resistivity [4,5]. The dependence of minority carrier lifetime on the doping concentration is often attributed to change in activity of the recombination centers due to the change in Fermi level position [4]. The lifetime degradation is associated with the existence of defects such as dislocations or precipitates that are introduced during crystal growth or device processing. To achieve low-cost high-efficiency solar cells, manufacturable gettering and passivation techniques should be developed to improve diffusion length in excess of twice the thickness of the substrate. Thin dendritic web silicon ribbon not only relaxes the requirement for high diffusion length but also reduces the cost of silicon material in the cells.

This paper shows, a) the effectiveness of phosphorus gettering during the lamp-heated belt furnace processing (BFP) and b) the combined effect of phosphorus gettering followed by simultaneous Al gettering and SiN-induced hydrogenation on the bulk lifetime of n-type, antimony doped dendritic web silicon. In addition, understanding and optimization of belt furnace gettering and passivation is used to achieve high efficiency screen-printed FSF PhosTop cells on n-type web and FZ silicon.

Experimental

A. As grown lifetime measurements

Six different resistivities (0.32, 0.57, 1.2, 2.2, 9.1 and 20.0 Ω -cm) of n-type, antimony doped dendritic web silicon were obtained from single ribbon pull to eliminate the variability in feed stock and growth run. The samples were cleaned in 1:1:2 $H_2SO_4:H_2O_2:H_2O$ for five minutes followed by a 3 minute rinse in DI water. This was followed by a clean in 1:1:2 $HCl:H_2O_2:H_2O$ for 5 minutes and a 3 minute rinse in DI water. A final dip in 10% HF for 2 minutes was performed followed by 30 seconds DI water rinse. The samples were then used for the as grown lifetime measurements by photo-conductance decay (PCD) technique. During the lifetime

measurement, the samples were placed in a 0.001M iodine in methanol solution to provide effective surface passivation.

B. Phosphorus Gettering and Passivation of web in the Belt Furnace

After the as-grown lifetime measurements, the samples were cleaned as above. Each sample was divided into 2 parts to study (a) phosphorus gettering alone (set 1), and (b) combined effects of P and Al gettering as well as SiN hydrogenation (set 2). Samples were coated with phosphorus spin-on dopant and baked for 2 minutes on a hot plate set at 200°C. This was followed by a 6-minute drive-in at 925°C in a lamp heated belt furnace. After the diffusion, the phosphorus glass was removed in 10% HF followed by a quick rinse in DI water. This resulted in a sheet resistance of $\sim 45 \Omega/\square$. After the phosphorus gettering, 860Å thick PECVD SiN film with an index of ~ 2.0 was deposited at 300°C on samples in set 2. Then the Al paste was screen-printed on the backside of the samples in set 2 and baked for 2 minutes, followed by p-n junction formation at 860°C for 2 minutes in the belt furnace. Finally, samples in both the two sets were etched down to bare Si to measure the bulk lifetime.

C. Cell fabrication

FSF cells were fabricated on a 20 Ω -cm n-web and a 2 Ω -cm (111) n-type, FZ silicon. The cell fabrication included cleaning the samples in RCA1 and RCA2 solutions followed by front surface field formation by spin-on phosphorus, bake, and a 6-minute belt furnace diffusion at 925°C. This resulted in a 40-45 Ω/\square front surface diffusion with a junction depth of about 0.25 μm and peak concentration of 2.6×10^{19} atoms/cm³. After the phosphorus glass removal and DI water rinse, a single layer PECVD SiN antireflection coating was deposited on the front at 300°C. This was followed by screen-printing of Al on the back and a 2 minute drive-in at 860°C in the belt furnace to form the p-n junction. A silver grid was screen-printed on top of SiN and then fired through the SiN at 730°C. The cells were then tested after a short FGA at 400°C.

Results and Discussion

A. Model Calculation

Model calculations in Fig. 1 show that for high efficiency 100 μm thick n-type FSF cell, a 60 μs lifetime is required to achieve greater than 14% efficient cells. This lifetime corresponds to a hole diffusion length (L_p) which is 2.5 times the thickness (W) of the substrate. Notice that for a 100 μm thick FSF cell, efficiency becomes relatively insensitive to lifetime above 60 μs . Model calculations indicate that a diffusion length of 285 μm ($\tau = 67 \mu\text{s}$) would be sufficient to achieve the maximum efficiency of $\sim 15\%$ for planar screen-printed FSF cell on 2 to 20 Ω -cm substrates. High resistivity cells give high short circuit current but lower fill factor, resulting in similar efficiency.

B. Doping dependence of As-Grown lifetime in dendritic web silicon

As shown in Figure 2, the as-grown lifetime in this particular web crystal growth run was found to be very low ($<1 \mu\text{s}$) for all the resistivities. However, the as-grown lifetime seems to be somewhat higher for higher substrate resistivity. The low as-grown lifetime could be due to the stress-induced recombination-active structural defects (dislocations) which are concentrated in the inner part of the substrate, particularly at and near the twin planes [4]. The structure of these dislocations or precipitates at the twin plane is believed to be more complex than simple dislocations because the simple and clean dislocations, at room temperature, are generally not active [6]. It could also be due to the quenched-in point defects during the growth. Note that the absolute values of the very low as-grown lifetime could have some error because of the PCD tester limit.

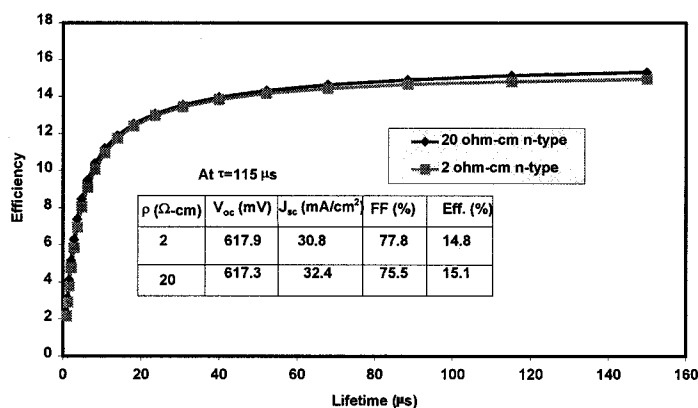


Fig. 1: PC-1D model calculation showing efficiency of n-type FSF cells as a function of bulk lifetime and base resistivity

C. Effect of Phosphorus gettering on n-type dendritic web silicon

Phosphorus gettering alone enhanced the minority carrier lifetime for all the resistivities (Fig. 3). For example, a lifetime of 0.99 μs for 20 $\Omega\text{-cm}$ web silicon increased to 5.4 μs , approximately a six-fold increase. However, the highest improvement in the lifetime due to P gettering alone was observed for the 9.1 $\Omega\text{-cm}$ web where the lifetime increased to a value of 15 μs from 0.92 μs . Even though phosphorus gettering alone is quite effective in gettering the impurities and defects in n-web, lifetime enhancement is not enough to achieve ~15% web cell (Fig. 1). This provided the motivation for investigating the combined effect of phosphorus and aluminum gettering in conjunction with PECVD SiN induced hydrogenation.

D. Combined effect of Phosphorus gettering and simultaneous Al and SiN heat treatment

Fig. 3 shows that the combined effect of phosphorus gettering followed by simultaneous Al and SiN heat treatment at 860°C for 2 minutes resulted in a very significant improvement in lifetime with 9.1 $\Omega\text{-cm}$ resistivity web reaching a lifetime value of 443 μs . Even the lowest resistivity substrate improved to 87 μs from 0.48 μs . It should be noted that the temperature cycles (925°C/6 min for phosphorus diffusion, 860°C for 2 minutes for Al diffusion and 730°C for 30 seconds for contact formation) used in this study simulate the front surface field diffusion, screen-printed Al p-n junction formation, and contact firing cycles during the actual cell fabrication. Therefore, the measured lifetime after all the treatments in Fig. 3 represents the lifetime value in the finished device. It was found that the final lifetime or diffusion length for all the resistivities was in excess of 70 μs , which is adequate to achieve high efficiency solar cells as predicted by the model calculations in Fig. 1.

E. High Efficiency FSF cells fabricated on n-type web and float zone silicon

Figures 4 and 5 show the measured and calculated IQE and cell data for the high efficiency FSF cells achieved, on web and FZ silicon, respectively. Detailed analysis of the IQE curve in Fig. 4 for the 14.2% efficient, 4 cm^2 web cell, gives a hole lifetime of 115 μs (L_p of 373 μm) with an effective S_{front} value of 80 cm/s at the n^+n interface. For the 14.9% n-type FZ cell in Fig. 5, a lifetime of over 200 μs (L_p of 492 μm) gave a good match between the calculated and for the experimentally measured IQE. The fill factors for both cells also matched the values predicted by the model calculations for the two resistivities. Even though, an efficiency of 15.1% is predicted for the 115 μs lifetime n-web (Fig. 1), only 14.2% was achieved experimentally. This may be the result of some non-uniformity in the S and lifetime values. Efforts are underway to push the screen-printed 100 μm thick FSF n-web cell efficiency to 15%.

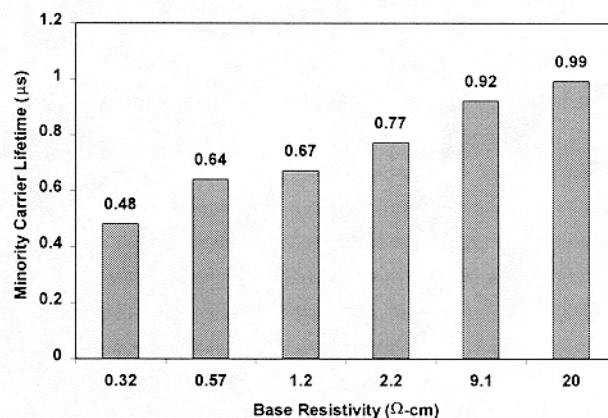


Fig. 2: Resistivity dependence of As-grown lifetime in n-type dendritic web silicon.

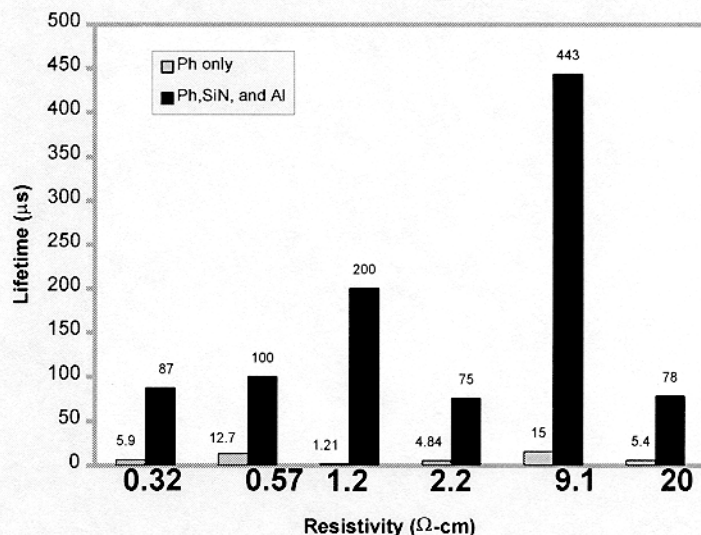


Fig. 3: The effect of phosphorus gettering, aluminum gettering, and SiN hydrogenation on the lifetime of n-web material for various resistivities.

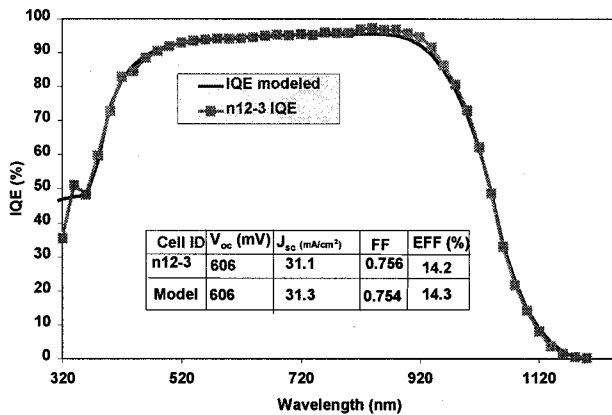


Fig. 4: Modeled and measured IQE for the High efficiency screen-printed PhosTop cell fabricated on 20- Ω -cm, 100 μ m thick dendritic web silicon.

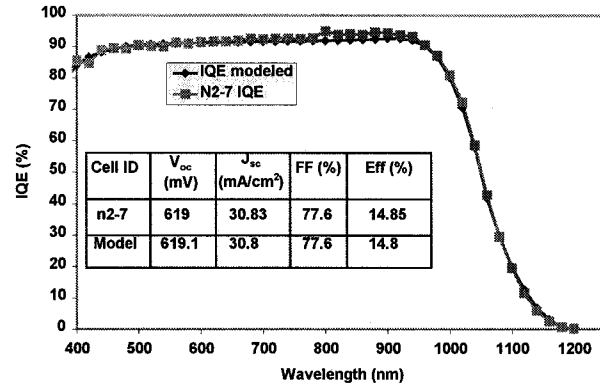


Fig. 5: Modeled and measured IQE for the High efficiency screen-printed PhosTop cell fabricated on 2 Ω -cm, 200 μ m thick FZ (111) silicon.

Conclusion

The as-grown lifetime in the n-type (antimony doped) dendritic web was found to be quite low and resistivity dependent. The low as-grown lifetime can be attributed to the quenched-in point defects during growth and/or dislocations accumulated near the twin boundaries about midway through the ribbon thickness. In order to improve the lifetime for high efficiency silicon solar cells, low cost gettering techniques using lamp-heated belt furnace were employed. Unlike the as-grown web, the lifetime in the processed n-web did not show any clear doping dependence due to the effective belt furnace gettering and passivation. P gettering alone was quite effective resulting in a lifetime of 15 μ s for the 9.1 Ω -cm web. The combined effect of P and Al gettering and SiN hydrogenation resulted in a lifetime in excess of 400 μ s for the 9.1 Ω -cm web. The combined effect raised the lifetime of all the resistivities above 70 μ s, which is required to achieve 14-15% efficient screen-printed FSF cells. The huge improvement in lifetime is attributed to the fact that Al alloying creates vacancies, which facilitates the dissociation of molecular hydrogen and enhances the incorporation of atomic hydrogen into the bulk. This results in enhanced passivation of defects. Lifetimes over 100 μ s were obtained, which endorses the use of the belt furnace for effective gettering and passivation in order to achieve ~ 15% efficient screen-printed FSF cells in thin silicon ribbon.

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Automation of the String Ribbon Process

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ABSTRACT

A method for producing crystalline silicon ribbon grown in a continuous process known as String Ribbon is now undergoing automation. A newly designed String Ribbon machine and some automated features it contains are described.

1. Introduction

Evergreen Solar is now commercializing a vertical silicon ribbon growth method termed String Ribbon. String Ribbon [1,2] produces silicon ribbon in a process illustrated in Figure 1.

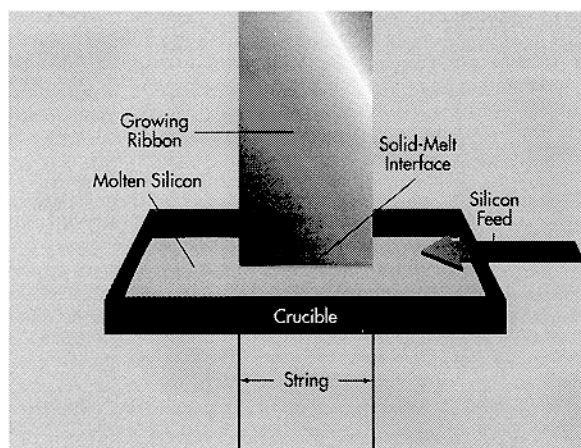


Figure 1 The String Ribbon Process

Spools of high temperature string material are used to feed the strings continuously to provide edge stabilization for the growing ribbon.

The String Ribbon process is an inherently robust one wherein the ribbon is grown on a continuous basis, 24 hours a day, by production operators. Machine throughput is then determined by the speed of growth and the ribbon width. For a 10 MW plant, Evergreen is planning on installing 120 ribbon machines according to the new design described below. The ribbon will be initially be 300 μm thick and 8 cm wide. In a separate research and development program, Evergreen Solar has developed the

technology to grow 100 μm , 8 cm wide ribbon. This will be introduced into our production line as a future generation technology.

2. New Furnace Design

The ribbon machine was completely redesigned in order to facilitate automation and operator productivity, and to reduce the capital cost per machine. While the size and cost of an individual machine of the present earlier design was small in comparison to any other known ribbon techniques, the drive to lower costs even further was behind this redesign effort. A photograph of the new machine is shown in Figure 2.

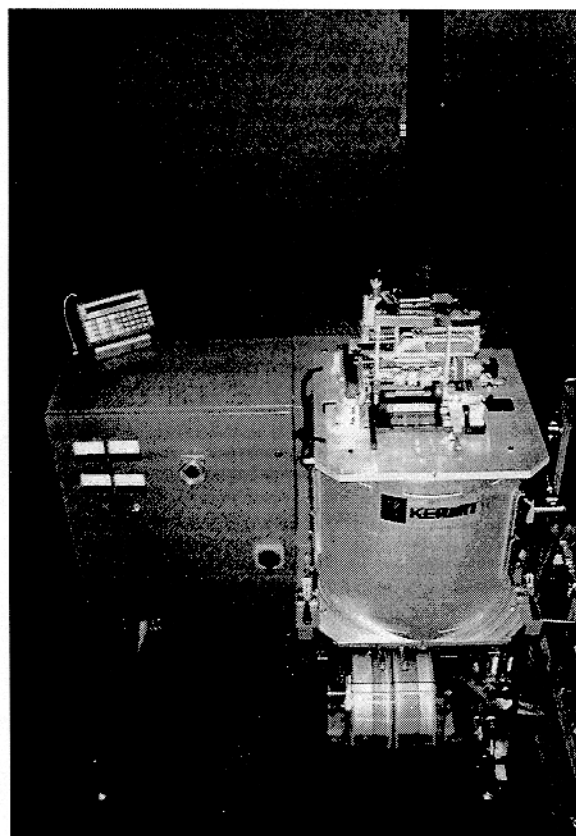


Figure 2 Furnace with ribbon growing from the machine.

The newly designed machine has these features: the outer, water cooled chamber, is 1/3 the cost of the previous machine; all the feedthroughs and access openings are now

much more tightly sealed; the feeder for the continuous supply of the feedstock silicon is more compact; the spool size for the strings has been enlarged such that spools are changed about ten times less frequently; all controls are run from a single PLC that can be interfaced with a central computer; viewports have been enlarged to make the machine more user friendly; growth of wider ribbon can be accommodated quite readily; and the overall machine cost is within the target of 20% lower than the previous machines.

3. Automation of Measurement and Control

At present, ribbon that is grown and used for our production line is 300 μm thick. Uniformity of ribbon thickness across the width of the growing ribbon is important for high yields. Prior to this work, thickness and melt depth were measured manually and temperature and feed rate adjustments were made manually when warranted based on operator input.

4. Automatic Melt Height Measurement and Control

The method for the automation of melt height measurement is based on the electrical properties of silicon and graphite. This technique allows the melt height to be determined continuously and without disturbing the melt. A non-linear voltage as a function of melt height is generated by this method, and a simple calibrated curve fit on this data, as shown in Figure 3, allows for the melt height to be determined automatically.

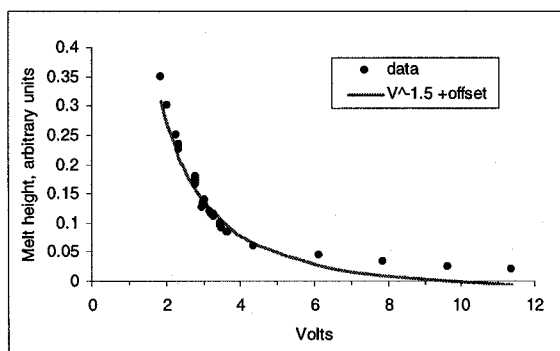


Figure 3 Melt height as a function of output voltage.

The melt height can then be controlled using a standard PID loop on an industrial PLC, which controls the rate of replenishment feed that is added to the system. This process can be controlled by a PID loop without difficulty during growth, because the range of melt height (output

voltage range of 1-2 volts) is approximately linear within the growth regime.

5. Automatic Thickness Measurement and Control

The next task in the automation project was the design and implementation of a non-contact automatic thickness measurement system. This method was found to improve repeatability and substantially reduce the standard deviation of the thickness measurement in comparison to the manual procedure. The new system also found subtle variations in the growing ribbon which were not able to be detected via manual measurement of the ribbon.

A subsequent task was to develop an algorithm for controlling ribbon thickness. Ribbon thickness is typically maintained by manually varying the inputs to the system (elements which modify the thermal environment of the system), in response to the outputs of the system (the thickness of the ribbon taken intermittently by hand at three points).

In order to automate this process, a model of how the system reacted at each of the output points as a function of each input was developed. An objective process function was also created based on the outputs (the thickness of the ribbon at three points) and the desired target thickness; this function minimizes as the process improves towards the target thickness. The model, coupled with the objective process function, allowed the prediction and ranking of which input changes would achieve the best output. By implementing this prediction and ranking scheme on a programmable logic controller (PLC), control changes were then made to the system in a consistent manner.

Figure 4 shows the thickness of the ribbon changes with time, and Figure 5 shows how the objective function is reduced during the automatic control of a furnace.

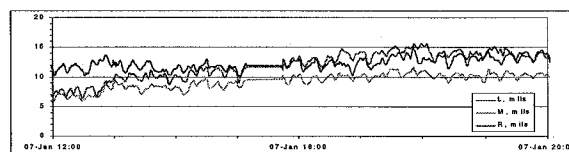


Figure 4 Thickness of the left, middle and right part of the ribbon under automatic control.

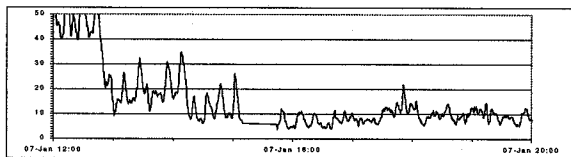


Figure 5 The objective function decreases to a minimum under automatic thickness control.

Finally, it should be noted that the automation of melt height and ribbon thickness measurement and control will facilitate the growth of 100 μm ribbon.

Summary

A new ribbon growth machine has been successfully operated in production and will be replicated in Evergreen's new factory. Automation of ribbon thickness control has been attained for this furnace.

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Interface States and H (D) Passivation at Si-SiO₂ Interface

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Abstract

An overview of the hydrogen passivation at the Si-SiO₂ interface is presented here. Hydrogen is found to passivate and depassivate the interface simultaneously, though dangling bond passivation is dominant at room temperature. Hydrogen can induce extra defects under certain conditions, and cause device degradation under hot carrier stress test. An alternative method of using deuterium instead of hydrogen in the passivation process has been shown to improve the interface hardness. The application of hydrogenation to Metal Insulator Semiconductor (MIS) solar cells are summarized.

I Introduction

A thin tunneling oxide between silicon and a semitransparent metal is known to lead to an increase in the built-in potential and in turn to an enhancement in the open circuit voltage in Metal-Insulator-Semiconductor (MIS) solar cells [1-4]. This MIS structure is an alternative to the conventional p-n junction devices. The maturity of this technology is due to a better understanding of the instabilities near the Si-SiO₂ interface, including the charges and surface states in thermally oxidized silicon. In a practical MIS diode, there exist many states and charges, which will affect the ideal device characteristics. They can be classified [5] as: Q_{ss} , fixed surface state charge; Q_0 , mobile impurity ion; N_{st} , fast surface states and N_{ot} , radiation induced charge. Q_{ss} is a positive, stable charge in the oxide, very close to the Si-SiO₂ interface. It cannot be charged or discharged by varying the silicon surface potential. Fixed surface-state charge is believed [5] to result from a nonstoichiometric silicon-oxygen structure in the Si-SiO₂ interface region, where the silicon atoms are excessive or oxygen is deficient. In either case, a positive charge results. Interface states have been studied over a long period of time. Historically, interface states are also known as fast states, or surface states. The so-called fast states derive their name from the fact that the traps responsible are in direct electrical communication with the silicon and, thus, respond rapidly to changes in surface potential. Interface states are located at the Si-SiO₂ interface and are characterized by energies within the silicon bandgap. Different from Q_{ss} , the fast surface states, N_{st} , can be charged or discharged by changing the silicon surface potential. The conventional Capacitance-Voltage (C-V) method or modern third-level charge pumping method can be used to obtain a measure of the state density in the band gap. It has been noted that fast state densities are generally initially proportional to Q_{ss} and thus also depend on silicon orientation. Fig 1 [6] shows the relationship between the two. Fu and Sah [7], Werner [8] and Breed and Kramer [9] have reported an apparent correlation between oxide fixed charge density and interface state density. This correlation indicates that oxide fixed charge and interface states

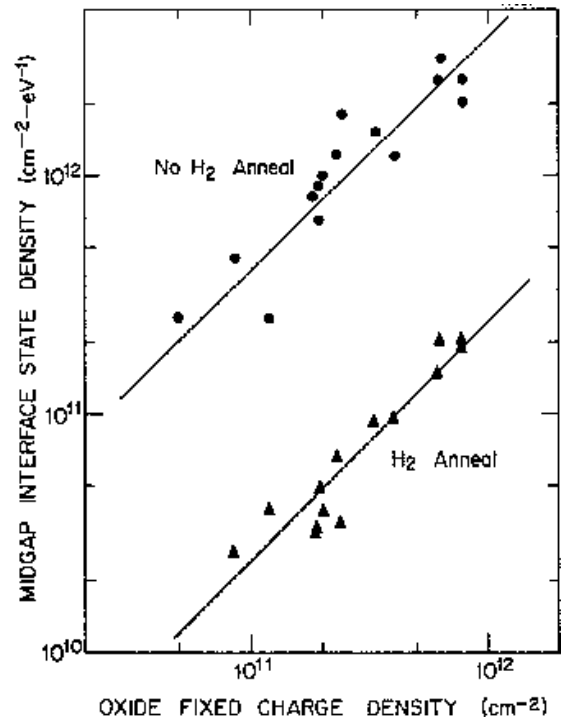


Fig. 1. Midgap interface state density vs. oxide fixed charge for annealed and H₂-annealed n-type and p-type silicon samples (100) and (111) orientation, oxidized in dry O₂ at 1000° and 1200°C. (Hydrogen anneal: 2 liters/min, 10% H₂ in N₂, 10 min, 500°C.) (Ref. 6).

may have a common origin. Fig. 1 contains a plot of oxide fixed charge density vs. midgap interface state density for samples with no post-oxidation hydrogen anneal as well as for samples which received a post-oxidation hydrogen anneal at 500°C for 10 min in a 10% hydrogen in nitrogen ambient.

At least three type of interface states have been identified [10,11]: The first type is intrinsic to the Si-SiO₂ system and believed [5] to be due to the interruption of the periodic lattice structure at the surface of a crystal. A second type of interface state is caused by ionizing radiation and generally anneals in nitrogen ambient at about 350°C. Upon exposure to ionizing radiation, a silicon-oxygen bond in the oxide may be broken (or it may already be broken) and holes formed by electron-hole generation are trapped at the silicon defect. At the same time, a silicon-oxygen bond at the silicon surface is broken, leading to fast state formation. The third type of Interface state has been associated with the presence of heavy metals at the Si-SiO₂ interface. These states are not normally annealable at temperatures below 500°C. Due to the rapid exchange of charges between the interface states and the silicon, the actual charge in the states at a particular instant

depends on the energy distribution of the states, the nature of the states (donor-like or acceptor-like), and the position of the Fermi level in the bandgap. The presence of exclusively donor-like states in the bandgap will always result in a net positive charge associated with the surface states which in turn will lead to a negative shift in the C-V curve for both p-type and n-type silicon. The presence of exclusively acceptor-like states in the bandgap will, on the other hand, result in a negative charge being associated with the interface states, which will shift the C-V curve toward more positive voltages. Fig. 2 shows such a capacitance stretch-out due to the interface states [10]. The extent of the shift and/or any frequency dispersion in the C-V curve will depend on both the location and magnitude of the states in the bandgap.

Either the capacitance measurement or the conductance measurement technique can be used to evaluate the interface states. It can be shown that the conductance technique can give more accurate results for MIS diodes with relatively low interface state density. Charge pumping (CP) techniques are powerful tools for characterization of the Si-SiO₂ interface traps especially in small geometry devices. Electron spin resonance (ESR) is perhaps the only spectroscopic tool that responds exclusively to defect atomic states in the Si-SiO₂ system.

II Interface States and Hydrogen

Though, obviously, hydrogen plays an important role in passivating the interface, the origin of the passivation and interface states is still a long story, which can be traced back into the oxidation step, that is, the relationship between D_{it} and Q_{ss} , and the dependence upon the final annealing step. A microscopic identification is needed to clarify the origin of the interface states, as well as the chemical kinetics of the hydrogen passivation behavior. We see that hydrogen can passivate the surface, but the reverse dissociation reaction proceeds in the mean time. Under certain circumstances, hydrogen can induce donor-type detrimental interface states.

In an early study of oxidized silicon wafers, Nishi [11] found three ESR centers, and subsequently determined their spectroscopic g factors to be 2.000 (isotropic), 2.000~2.010 (anisotropic), and 2.065

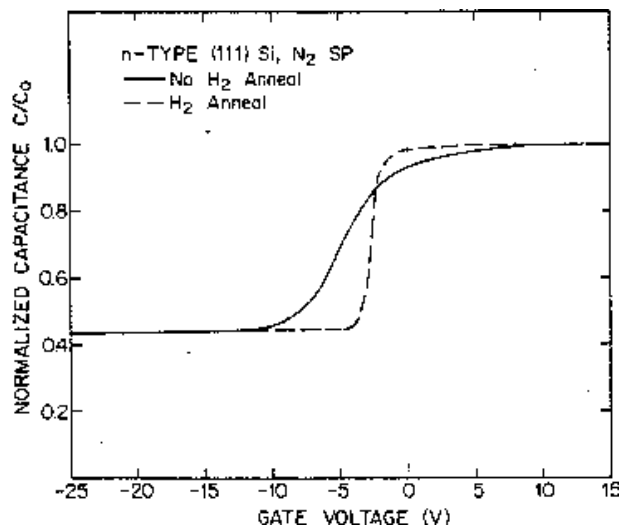


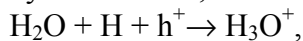
Fig. 2. High frequency C-V curves for non-H₂-annealed and H₂-annealed (500°C, 10% H₂ in N₂, 10 min) MOS structures in n-type (111) silicon, oxidized in dry O₂ at 1000°C and pulled in nitrogen. (Ref. 6).

(nearly isotropic). He assigned them as P_a , P_b , and P_c , respectively, and examined certain aspects of their behavior after different wafer-processing treatments. The P_c signal was later shown to be due to neutral elemental iron [12], and P_a resembles the signal from donor or conduction electron [13]. P_b appears to be most pertinent to the inherent defect structure of the interface. Caplan [14] has performed an extensive search for possible correlation of ESR centers with oxide fixed charge Q_{ss} or interface states N_{st} . Energy distribution of P_b centers and electronic traps (D_{it}) at the Si-SiO₂ interface in Metal-Oxide-Semiconductor (MOS) structure was first quantified by Poindexter [15] by ESR and C-V analysis. Wafers of (111)-oriented silicon were dry-oxidized for maximum P_b and trap density, and metallized with a large MOS capacitor for ESR and adjacent small dots for C-V measurements. Analysis of C-V data shows two D_{it} peaks. The ESR spin density reflects addition or subtraction of an electron from the singly occupied paramagnetic state and shows transitions in amplitude of about $1.5 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$ at $E_v + 0.31 \text{ eV}$ and $E_v + 0.80 \text{ eV}$. The correlation of electrical and ESR responses and their identical chemical and physical behavior are the further evidence that $\bullet\text{Si}=\text{Si}_3$ is a major source of interface electronic traps in the 0.15-0.95 eV region of the Si band gap in unpassivated material.

The first unified chemical kinetic model was proposed by Brower in [16] (1990), which involves the hydrogen chemistry of P_b centers. Before his work, a model for the chemical kinetics involving the passivation of P_b center at the (111) Si-SiO₂ interface was developed from ESR studies [15]. Cartier [17] found that the dangling-bond passivation dominate at room temperature, such that the P_b center can only account for a small fraction of the total number of electrically active interface defects produced by atomic hydrogen. No P_b resonance could be observed in the ESR samples before atomic hydrogen exposure. During the exposure to the atomic hydrogen, both the D_{it} and P_b are gradually induced by repetitive atomic hydrogen exposure. As total exposure time in hydrogen ambient increases, ΔD_{it} increases linearly, with no indication of saturation, while ΔP_b saturates at a value of $3\text{-}6 \times 10^{11} \text{ cm}^{-2}$. This verified the reversible passivation chemical reaction.

III Hydrogen Induced Interface States and Degradation

By setting optimal process conditions, hydrogen can dramatically reduce the interface states, and hence improve the device performance. It should be noted that hydrogen annealing is not only beneficial, but also can be detrimental under some conditions. Sah et. al. recognized some of these negative effects technologically early on [18]. They proposed an atomic model for the generation and annealing of three donor-like defects (the bulk compensating donor, the donor-like interface density-of-state (DOS) peak, and the positive turnaround charge) in MOS capacitors, which involved hydrogen release and migration to the Si-SiO₂ interface. Thus far, the P_b center has been considered as the primary candidate for the interface defect. Early experimental work has provided for a depassivation mechanism, but recent studies unambiguously demonstrate that considerably larger numbers of centers of a different nature can be generated at the same time. A large number of non- P_b -type centers can be generated when subjecting a MOS system to Fowler Nordheim [19] stressing or by hole annihilation [20,21]. Cartier *et al.* showed that exposition of a bare Si/SiO₂ system to atomic H introduces up to 10^3 cm^{-2} of non- P_b -type centers. These centers anneal at room temperature when neutral but are stable when charged positively. Moreover, the anneal process is accompanied by the release of H. Nijs *et al.* [22] proposed that the donor states are related to H attached interfacial network sites, most likely O atoms. In analogy with the formation of the hydronium ion,



H attaches to O, leading to the formation of a $(\equiv\text{Si})_2=\text{O}\cdots\text{H}$, an electrically active complex. When positively charged, H is strongly bonded; when neutral H is only weakly attached. In the latter case, it can escape and dimerize so that the states disappear. Recently, hydrogen enhancement of thermally induced interface degradation was demonstrated by Stesmans [23]. The process of interface degradation induced in (111) Si/SiO₂ by postoxidation annealing (POA) in vacuum, previously identified by ESR as creation of persistent P_b centers, is found to be strongly enhanced (≈ 6 times) when performed in H₂ ambient.

Additionally, as sensed by ESR, the threshold temperature for creation is lowered from $\approx 640^\circ\text{C}$ for vacuum to $\approx 550^\circ\text{C}$. It is important to emphasize that hydrogenation does not definitely remove the P_b defect entity: the physical density [including both the unpassivated ESR-active ones (P_b) and those passivated by H (P_bH) or some other means (P_bX)] remains unaltered. While thus well masked by the H passivation, the threat to technology is clear: during device operation, knock off of H will result in electrical reactivation of P_b defects, the devices thus getting more vulnerable to hot electron (hole) stressing and irradiation. The degradation mechanism consists of interfacial $\text{Si}(\text{O})$ bond rupture resulting in permanent creation of substantial number of P_b centers in addition to the unavoidable inherent number N_0 in the as-oxidized states. The overexposure to H_2 should be avoided. Alternative methods of passivation may be of interest for understanding device degradation behavior in relation to hydrogen dissociation.

The idea of using deuterium instead of hydrogen was in part inspired by the experiments of hydrogen / deuterium desorption induced by the tip of scanning tunneling microscopy (STM). Replacement of hydrogen with deuterium during the final wafer sintering process later showed great reduction of hot electron degradation effects in MOS transistors [24-29]. Lyding *et al.* [30] conducted nanoscale patterning of hydrogen terminated $\text{Si}(100)\text{--}(2\times 1)$ surface, and found that patterning occurs when electrons field emitted from the probe locally desorb hydrogen. Avouris and coworker [31] later investigated the STM-induced H and D atoms desorption from the same surface, and showed the same energy threshold that corresponds to the excitation energy of the $\text{Si}\text{--}\text{H}(\text{D})$ group. The H desorption yield, however, is much higher than the D yield. As shown in Fig. 3, the D desorption yield is about 50 times lower than the H yield. Cryogenic UHV-STM studies of $\text{H}(\text{D})$ desorption was conducted by Lyding *et al.* [32]. The desorption shows no temperature dependence in the high energy electronic desorption regime. However, in the low energy vibrational heating regime, hydrogen is over two orders of magnitude easier to desorb at 11K than at room temperature. These results may have direct implication on low temperature operation of some devices such as CMOS circuits.

The time-dependent degradation of MOS transistor performance resulting from hot electron effects has been an area of considerable study over the past 30 years [33]. According to established theory, this aging process is thought to occur in part as the result of hot electron stimulating the desorption of hydrogen from the $\text{Si}\text{--}\text{SiO}_2$ interface region. Basic research on hydrogen interactions with semiconductors started more than 40 years ago. In 1956 Van Wieringen and Warmoltz [34] published their landmark experiments on permeation of hydrogen in single-crystal Si and Ge, producing values for hydrogen solubility and diffusivity that are still valid after all these years. Over the subsequent two decades, the conventional wisdom seemed to be that hydrogen interacted only weakly with the semiconductor. All this changed while attempting to understand the beneficial effects of hydrogen on the properties of amorphous silicon, and interaction of hydrogen with impurities. In Si, Pankove and coworkers [35] showed neutralization of shallow acceptor, while Johnson *et al.* [36] established passivation of shallow donors. These developments caused a veritable explosion in research activities relating to hydrogen in semiconductors, peaking in the early 1990's. Since 1996, however, we have witnessed a resurgence in interest due to the discovery of several phenomena and processes in which hydrogen plays a key role, and which have a profound impact on technology, such as the lifetime improvement due to deuterium processing.

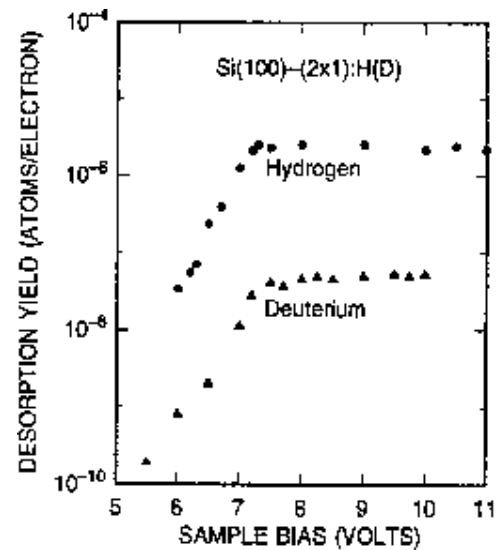


Fig. 3. Comparisons of the STM-induced desorption yields of hydrogen and deuterium from $\text{Si}(100)\text{--}(2\times 1)\text{:H}(\text{D})$ as a function of the sample bias voltage. (Ref. 31).

Strong bonds between hydrogen and host silicon atoms can be formed when disruption in the perfect crystal is present; for instance, at a surface, at an interface, in polycrystalline or amorphous material, or near a point defect in the bulk. The formation of such strong bonds between hydrogen and host atoms is often implicitly considered to be due to the passivation of dangling bonds. It is indeed often assumed that intrinsic deep levels are due to dangling bonds. Since H bonds more strongly to Si than Si to Si, it became evident that the energy gap of a-Si:H should be larger than that of crystalline Si (c-Si). This suggested to Pankove that hydrogenating the surface of c-Si would reduce surface recombination, since now the widened gap at the surface would form potential barriers that would repel both electrons and holes from the surface. This was verified experimentally by Pankove *et al.* [35]. Hydrogen not only passivates undercoordination defects (dangling bonds), but also interacts with overcoordinate defects. Indeed, in crystalline Si it has been accepted for some time that vacancies are not the only type of intrinsic defect to play a role [37]. Self-interstitials have formation energies comparable to those of vacancies [38]. In crystalline silicon, the self-interstitials are known to play a role in self-diffusion, impurity diffusion, surface reconstruction, planar interstitial defects, and dislocation nucleation [39]. First-principle calculations of complexes consisting of one or two H atoms and a Si self-interstitial were reported by

Van de Walle and Neugebauer [39]. It was found that hydrogen interacts strongly with self-interstitials; while the calculated binding energy is small for H interacting with a vacancy, it is large enough for the complexes to be stable at room temperature. The resulting energy is shown in Fig. 4. The electronic structure of the complex between a self-interstitial and one H atom indicates that it is amphoteric in nature, with the acceptor level located less than 0.1 eV above the donor level, both located around 0.4 eV above the valence band. The complex with two hydrogen atoms has no levels in the band gap, consistent with all the bonds being satisfied. The calculated vibrational frequencies for the Si-H stretch mode in these complexes are around 1900 cm^{-1} . These values are somewhat lower than for Si-H bonds at dangling bonds, which could help explain the absorption band broadening towards low frequencies. Hydrogen passivation of dangling-bond defects plays an important role in devices. Indeed, a hydrogen passivation step is part of all integrated circuit processing now. It ensures that the defect density at the Si-SiO₂ interface is low enough to meet the stringent specifications for device characteristics. However, during device operation or stress test, hot electrons can cause degradation of device parameters. Clearly, this is mainly due to the dissociation of Si-H bonds, leading to increased defect densities and hence a reduced lifetime. It is therefore important to have a thorough understanding of the dissociation mechanisms of the Si-H bond. The path followed by the hydrogen atom during the breaking of a Si-H bond plays a crucial role in the dissociation mechanism. Because deuterium is twice as heavy, it is anticipated that it does not accelerate as rapidly and the electrons return to the bonding state before dissociation can occur in the Si-H(D) bond.

While the influence of deuterium processing on the performance of silicon solar cells is not well understood, some success has been achieved with hydrogen passivation of MIS solar cells [1-4]. Hydrogen passivation of multi-crystalline silicon has been shown to increase cell efficiencies by about 5% to 7% [4]. The photovoltaic properties of p-n junctions solar cells have been shown to improve upon hydrogenation of polycrystalline silicon [2]. This has been attributed to reduction in the potential barrier

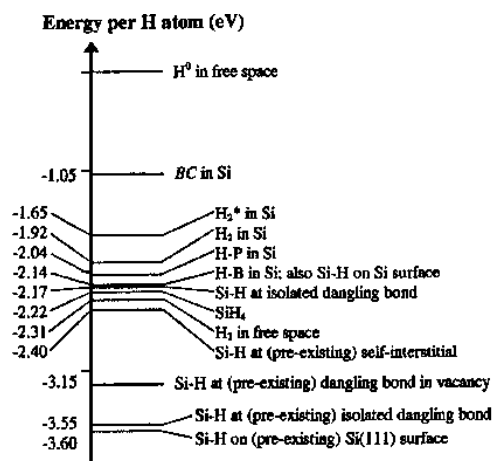


Fig. 4. First-principle energies for various configurations of H in Si. The zero of energy corresponds to a free H atom. The energy values were determined with first-principle pseudopotential-density-functional calculations, and include zero-point energies. (Ref. 40).

and minority carrier recombination at the grain boundaries in polysilicon based devices. Treatment of a-Si:H surface in a H₂O microwave plasma has led to a significant enhancement of V_{oc} in amorphous silicon MIS solar cells [1].

6 Conclusions

In the Si-SiO₂ system, annealing conditions have significant influence on the midgap interface-state density D_{it} and Q_{ss}, the fixed charge in thermal SiO₂. The partially ionized silicon plays an important part in charge and interface states formation. A dominant type of interface trap, P_b, was identified and quantified by ESR. The distribution of P_b in the band gap showed its correlation with D_{it}. The chemical behavior of hydrogen passivation at the Si-SiO₂ interface shows that a reverse reaction or depassivation process occurs spontaneously. The dangling-bond passivation is dominant at room temperature. However, the overexposure to H₂ should be avoided, since it induces extra amount of defects and causes a further degradation. The degradation of devices under stress test was found to be due to hydrogen release, which causes drifts in device parameters. Replacement of hydrogen with deuterium during the passivation process seems to enhance the interface hardness. However, further studies are required to substantiate the possible advantages of deuterium over hydrogen in silicon device technology. Results of utilization of hydrogen passivation in solar cells have been summarized.

Acknowledgements

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<p>13. ABSTRACT (<i>Maximum 200 words</i>). The 10th Workshop will provide a forum for an informal exchange of technical and scientific information between international researchers in the photovoltaic and non-photovoltaic fields. Discussions will include the various aspects of impurities and defects in silicon-their properties, the dynamics during device processing, and their application for developing low-cost processes for manufacturing high-efficiency silicon solar cells. Sessions and panel discussions will also review thin-film crystalline-silicon PV, advanced cell structures, new processes and process characterization techniques, and future manufacturing requirements to meet the ambitious expansion goals described in the recently released U.S. PV Industry Roadmap. The Workshop will also provide an excellent opportunity for researchers in private industry and at universities to recognize a mutual need for future collaborative research.</p> <p>The three-day workshop will consist of presentations by invited speakers, followed by discussion sessions. In addition, there will be two poster sessions presenting the latest research and development results. The subjects to be discussed include: solar cell processing, light-induced degradation, gettering and passivation, crystalline silicon growth, thin-film silicon solar cells, and impurities and defects. Two special sessions will be featured at this workshop: advanced metallization and interconnections, and characterization methods.</p>				
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